Agilent TS-5400 High Performance PXI Functional Test System

Diagnostics User's Guide

Agilent Technologies

Notices

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Table of Contents

List of Figures

List of Tables

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Any adjustment, maintenance, or repair of this product must be performed by qualified personnel. Contact your customer engineer through your local Agilent Service Center.

Agilent on the web

You can find information about technical and professional services, product support, and equipment repair and service on the web: http://www.agilent.com/

Double-click the link to **Test & Measurement**. Select your country from the drop-down menus. The Web page that appears next has contact information specific for your country.

Agilent by phone

If you do not have access to the Internet, call one of the numbers in the "Contact us" section at the end of this manual.

2
Safety and Regulatory Information

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies, Inc. assumes no liability for the customer's failure to comply with these requirements.

Safety Notices

CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like, that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

General Safety Considerations

This product is provided with a protective earth terminal. The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

WARNING

- **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE. Do not operate the product in the presence of flammable gases or flames.**
- **DO NOT REMOVE RACK PANELS OR INSTRUMENT COVERS. Operating personnel must not remove any rack panels or instrument covers. Component replacement and internal adjustments must be made only by qualified service personnel. Products that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by a qualified service personnel.**
- **The protection provided by the TS-5400 system may be impaired if the system is used in a manner not specified by Agilent.**

Environmental Conditions

The TS-5400 Automotive Electronics Functional Test System is designed for indoor use only. Table 2-1 shows the general environmental requirements.

Table 2-1 General environmental requirements

Environment condition	Requirement
Maximum altitude	2000 m
Operating temperature	5 °C to 40 °C
Relative humidity	5% to 80% relative humidity (non-condensing)

CAUTION This product is designed for use in Installation Category II and Pollution Degree 2, per IEC 61010-1 and 664 respectively.

Before Applying Power

Verify that the product is set to match the available line voltage and that all safety precautions are taken. Note the external markings of the instruments described in "Safety Symbols and Regulatory Markings".

Ground the System

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the AC power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses

Use only fuses with the required rated current, voltage, and specified type (normal blow, time delay). Do not use repaired fuses or short-circuited fuse holders. Doing so could cause a shock or fire hazard.

WARNING **To avoid electrical hazards, all system internal fuses must be replaced by trained and qualified personnel.**

Operator Safety Information

WARNING **Module connectors and test signal cables connected to them cannot be operator-accessible.**

Cables and connectors are considered inaccessible if a tool (such as a screwdriver, wrench, or socket) or a key (for equipment in a locked cabinet) is required to gain access to a conductive surface connected to any cable conductor (High, Low, or Guard).

WARNING **Ensure that the equipment-under-test has adequate insulation between the cable connections and any operator-accessible parts (doors, covers, panels, shields, cases, or cabinets.)**

Verify that there are multiple and sufficient protective means (rated for the voltages you are applying) to ensure that the operator will NOT come into contact with any energized conductor even if one of the protective means fails to work as intended. For example, the inner side of a case, cabinet, door cover, or panel can be covered with an insulating material as well as routing the test cables to the front panel connectors of the module through non-conductive, flexible conduit such as that used in electrical power distribution.

Safety Symbols and Regulatory Markings

Symbols and markings on the system, in manuals, and on instruments alert you to potential risks, provide information about conditions, and comply with international regulations. Table 2-2 defines the symbols and markings you may find in a manual or on an instrument.

Table 2-2 Safety symbols and regulatory markings

Symbol	Description
Safety symbol	
	Warning: risk of electrical shock.
	Warning: hot surface.
	Caution: refer to accompanying documents.
	Laser radiation symbol: marked on products that have a laser output.
	Alternating current.
	Both direct and alternating current.
	Three-phase alternating current.
	Earth (ground) terminal.
	Protective earth (ground) terminal.

Table 2-2 Safety symbols and regulatory markings

Symbol	Description
	Frame or chassis terminal.
	Terminal is at earth potential. Used for measurement and control circuits designed to be operated with one terminal at earth potential.
	Terminal for a neutral conductor on permanently installed equipment.
	Terminal for a line conductor on permanently installed equipment.
	Standby (supply); units with this symbol are not completely disconnected from the AC mains when this switch is turned off. To completely disconnect the unit from the AC mains, either disconnect the power cord, or have a qualified electrician install an external switch.
Regulatory marking	
	The CE mark is a registered trademark of the European Community. If it is accompanied by a year, it indicates the year the design was proven.
	The CSA mark is a registered trademark of the Canadian Standards Association.
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australian EMC Framework regulations under the terms of the Radio Communications Act of 1992.
ISM - 1A	This text indicates that the instrument is an Industrial Scientific and Medical Group 1 Class A product (CISPER 11, Clause 4).

Declaration of Conformity

The Declaration of Conformity (DoC) for this instrument is available on the Agilent website. You can search the DoC by its product model or description at the web address below.

http://regulations.corporate.agilent.com/DoC/search.htm

NOTE If you are unable to search for the respective DoC, contact your local Agilent representative.

Electrostatic Discharge (ESD) Precautions

Static electricity is destructive to your production process and the TS-5400. Careless handling and poor site planning can cause system reliability problems and reduce your product yield. The system may not be as easily damaged as the modules you will be testing, but good anti-static planning will help ensure high reliability.

The ESD symbol below indicates areas where ESD caution must be exercised. This is to prevent damage to instruments and/or test disruption.

Caution: static sensitive

Electrostatic discharge in this area may cause equipment damage and/or test disruption.

While not an exhaustive list of anti-static precautions, Table 2-3 provides suggestions to consider as you plan your system area.

Table 2-3 Suggested anti-static solutions for site planning

Precaution	Suggested solution
Anti-static flooring	Plan to use an anti-static floor covering or mats.
Grounding straps	Plan for foot straps in conjunction with anti-static flooring and wrist straps for system operators.

CAUTION

The system test rack is secured to the pallet of the shipping crate and wrapped with a plastic wrap. Do not move the crate or the test rack and pallet to a static-sensitive area until you have removed the plastic wrap from the test rack.

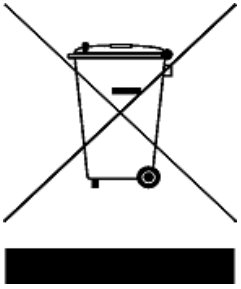
End of Life: Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC

This instrument complies with the WEEE Directive (2002/96/EC) marking requirement. This affixed product label indicates that you must not discard this electrical or electronic product in domestic household waste.

Product Category:

With reference to the equipment types in the WEEE directive Annex 1, this instrument is classified as a "Monitoring and Control Instrument" product.

The affixed product label is as shown below.



Do not dispose in domestic household waste.

To return this unwanted instrument, contact your nearest Agilent Service Center, or visit

www.agilent.com/environment/product

for more information.

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3
Running Diagnostics

This chapter describes the overview of the diagnostic testplans, the DGN testplan, and the CEDGN testplan. It also teaches you to use the diagnostics test fixtures to verify the operation of the system equipment.

NOTE Diagnostic testing is intended to verify basic connectivity and instrument functionality. It does not provide a full functional test of instrumentation and specifications.

Overview of Diagnostics Testplans

Standard diagnostic testplans are shipped with each system. There are two different testplans to test the system, from functionality to internal connections, to connections on the Test System Interface (MACPANEL).

The first testplan, called the DGN, is used to verify both the core system instrument operation and internal test paths. No hardware is required to run this testplan. It verifies about 50% of the system functionality.

The second testplan, the “Customer Engineer Diagnostics” testplan or simply CEDGN, is used to complete the test coverage. This test requires external hardware, which is packaged as a CEDGN kit, because it verifies the internal connections out to the Test System Interface.

The tests are executed in the Agilent TestExec SL software and the TS-5000 system programming environment using both standard and specialized test actions. The testplans only cover standard instruments in the system. If there is a special case where non-standard equipment are incorporated into the system, tests for these equipment would have to be added.

Standard instruments and the system.ust file

Before running the DGN or CEDGN testplans, instruments in the system have to be added to the *system.ust* file. Testplans can access and control instruments only if they have been added into the *system.ust* file.

Standard instruments in the TS-5400 are included in the DGN and CEDGN testplans. A ✔ (tick) next to an instrument shows that it is included in the DGN or CEDGN testplan.

Table 3-1 List of standard instruments in the TS-5400 system

P/N	Description	DGN	CEDGN
E6198B	21-Slot Switch/Load Unit	✔	✔
E8782A	40 Measurement Channels and 24 Instrument Channels Matrix Card	✔	✔
E8783A	64-Pin Matrix Card	✔	✔
E6175A	8-Channel Load Card		✔
E6176A	16-Channel Load Card		✔
E6177A	24-Channel Load Card		✔
E6178B	8-Channel Load Card		✔
U7177A	24-Channel Load Card with Current Sense		✔
U7178A	8-Channel Heavy Duty Load Card		✔
U7179A	16-Channel High Current Load Card		✔
N9377A	16-Channel Dual-Load Load Card		✔
N9378A	24-Channel Low Resistance Load Card		✔
N9379A	48-Channel High-Density Load Card		✔
M9018A	PXI Chassis		
M9021A	PCI Cable Interface		
M9182A	DMM	✔	✔
M9183A	DMM	✔	✔
M9186A	V/I Source	✔	✔
M9185A	8-Channel/16-Channel DAC	✔	✔
M9216A	32-Channel HV-DAQ	✔	✔
L4534A	4-Channel Digitizer	✔	✔
33522A	2-Channel Arbitrary Waveform Generator	✔	✔
N3300A	Electronic Load Mainframe	✔	✔
N6702A	1.2 kW, 4-Slots Modular Power Supply Mainframe	✔	✔

Table 3-1 List of standard instruments in the TS-5400 system

P/N	Description	DGN	CEDGN
N6700B	400 W, 4-Slots Modular Power Supply Mainframe	✔	✔
N6756A	DC Power Module N6756A - 60 V, 17 A, 500 W (2-Slots)		✔
N6752A	DC Power Module N6752A - High Performance, 50 V, 10 A, 100 W		✔
N6751A	DC Power Module N6751A - High Performance, 50 V, 5 A, 50 W		✔
N6762A	DC Power Module N6762A - Precision, 50 V, 3 A, 100 W		✔
N6761A	DC Power Module N6761A - 50 V, 1.5 A, 100 W		✔
N6734A	DC Power Module N6734A - 35 V, 1.5 A, 300 W		✔
N6773A	DC Power Module N6773A - 20 V, 15 A, 300 W		✔
N6774A	DC Power Module N6774A - 35 V, 9 A, 300 W		✔
N6775A	DC Power Module N6775A - 60 V, 5 A, 300 W		✔
N6776A	DC Power Module N6776A - 100 V, 3 A, 300 W		✔
N5764A	Power Supply, 20 V, 76 A, 1520 W		✔

Configuring the system.ust file in the System Configuration Editor

1 Start the System Configuration Editor by clicking this icon on your desktop:

2 Click on the *detected on system* button. The screen will show instruments detected on the system. Any instrument in Table 3-1 which is in your system should be detected.

3 Double-click on the instrument name to add it to the *system.ust* file. It is recommended that you add instruments in the following order:

i the first SLU,

ii the first pin matrix card in the first SLU, and

iii other instruments in any order.

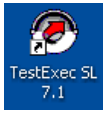
NOTE At least 1 SLU, 1 Pin Matrix, and 1 DMM must be in the system and in the *.ust* file for the DGN and CEDGN testplans to run.

4 Once the instruments have been added, click **Save** or **Save As** if you would like to change the name of your *.ust* file.

NOTE Ensure that you have added all the standard instruments you would like to test. The DGN and CEDGN testplans will only test instruments in the *.ust* file.

Configuring and Running the DGN Testplan

1 Start the Agilent TestExec SL (version 7.1 or greater) by clicking this icon on your desktop:



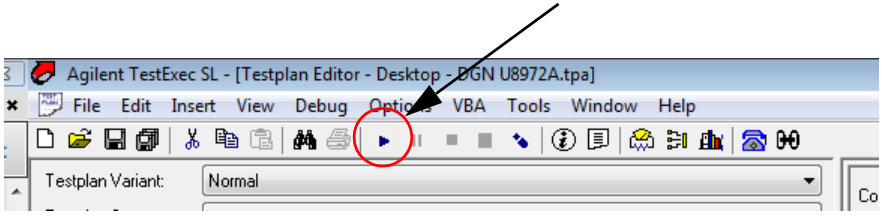
2 Load the *DGN U8972A.tpa* testplan into the TestExec SL. The testplans are located in this directory:

```
C:\Program Files\Agilent\TS-5000 System
Software\testplan\dgn
```

or

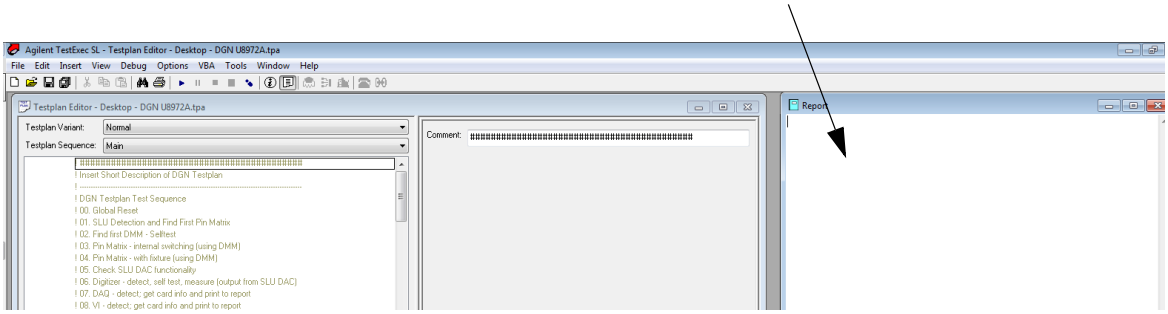
```
C:\Program Files (x86)\Agilent\TS-5000
System Software\testplan\dgn
```

3 Press the play button (shown by the arrow in the figure below) to run the testplan.



4 During certain sequences, message boxes will pop up with instructions on putting on fixtures or taking them out. Follow these instructions carefully to avoid any test errors.

5 The test report will be printed in the report window (shown by the arrow in the figure below).



Configuring and Running the CEDGN Testplan

1 Start the Agilent TestExec SL (version 7.1 or greater) by clicking this icon on your desktop:

2 Load the *CEDGN U8972A.tpa* testplan into the TestExec SL. The testplans are located in this directory:

```
C:\Program Files (x86)\Agilent\TS-5000
System Software\Service\U8972A\Testplans
```

or

```
C:\Program Files (x86)\Agilent\TS-5000
System Software\Service\U8972A\Testplans
```

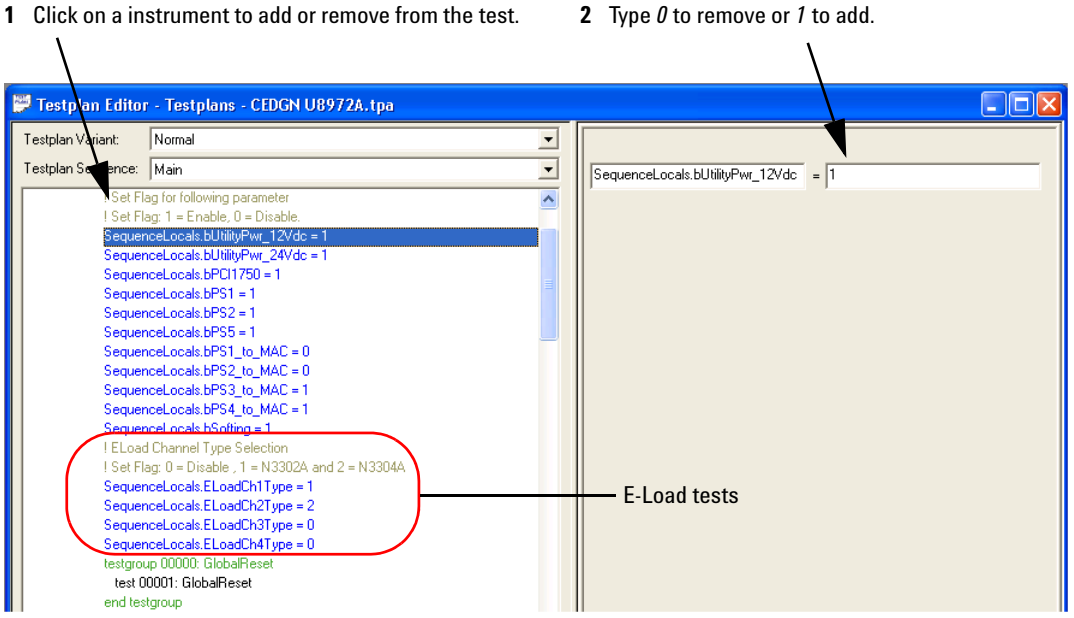
3 The CEDGN testplan will perform the test according to the settings set in the system topology file.

However, there are a few hardwares and instruments (Utility Power Supply +12 V, Utility Power Supply +24 V, PCI1750 (PCI DIO), DUT Power Supply, Softing CAN, and E-Load) that also needs to be configured in the CEDGN testplan as shown in Figure 3-1.

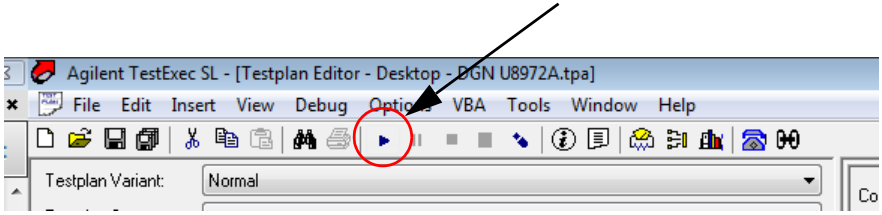
Place a *1* next to instruments you want to test and a *0* next to the instruments you do not want to test (or instruments that are not in your system).

For E-Load testing, identify the E-Load model in the testplan by placing a *1* next to E-Load module if it is a N3302A, a *2* next to E-Load module if it is a N3304A, or a *0* to ignore the test.

Figure 3-1 Specify the instruments to be tested in the CEDGN testplan



4 Press the play button (shown by the arrow in the figure below) to run the testplan.



The testplan will run tests on each instrument configured in the system topology file and also the instruments specified in step 3. The results of the tests are displayed.

5 Follow the instructions appearing on the display throughout the test.

Installing the Diagnostic Test Fixtures

Specific diagnostic test fixtures are required to be connected to the Test System Interface based on the message prompted while running the CEDGN testplan. The DGN testplan only requires external fixture connection for Pin Matrix Card tests, whereas the CEDGN testplan would most likely require more types of fixtures. The number of fixtures required would depend on the instruments installed in the system.

Figure 3-2 shows the Universal CEDGN Test Fixture U8972-67901 connected to the Pin Matrix's slot (1-4 and 6-9) with CEDGN Pin Matrix Cable U8972-61625. This fixture connection is used to test the connectivity and Pin Matrix functionality. This fixture is the only one required for DGN tests.

Figure 3-2 Installing a Universal CEDGN Test Fixture U8972-67901 with a CEDGN Pin Matrix Cable U8972-61625

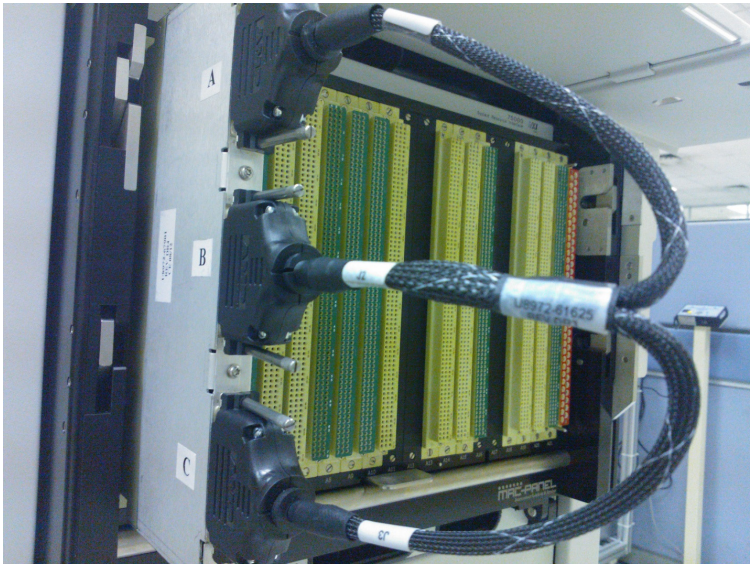


Figure 3-3 shows a Universal CEDGN Test Fixture U8972-67901 connected to Slot 1 and another Universal CEDGN Test Fixture U8972-67901 connected to Slot 10.

The CEDGN System Utility Cable U8972-61627 is used to link the two Universal CEDGN Test Fixtures U8972-67901 together. This fixture connection is used to test the connectivity, system utility functionality, and instrument functionality.

Figure 3-3 Installing two Universal CEDGN Test Fixtures U8972-67901 with a CEDGN System Utility Cable U8972-61627

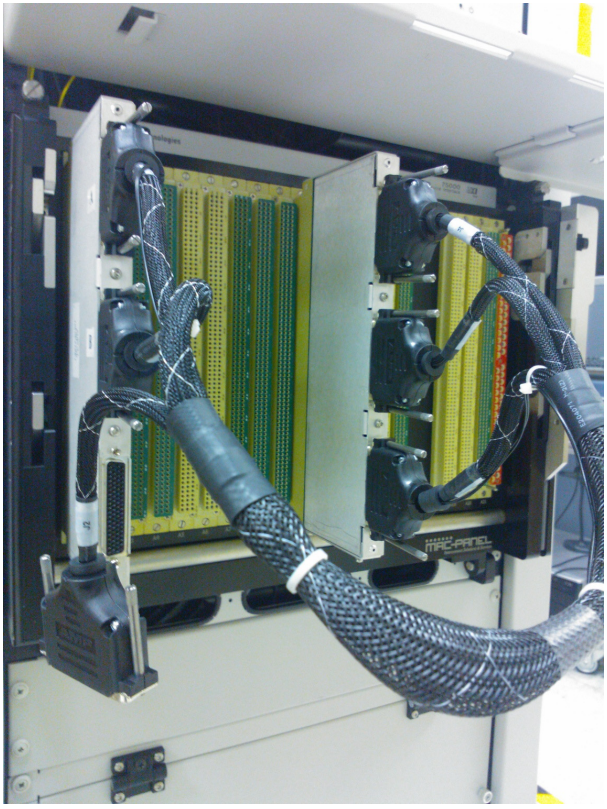
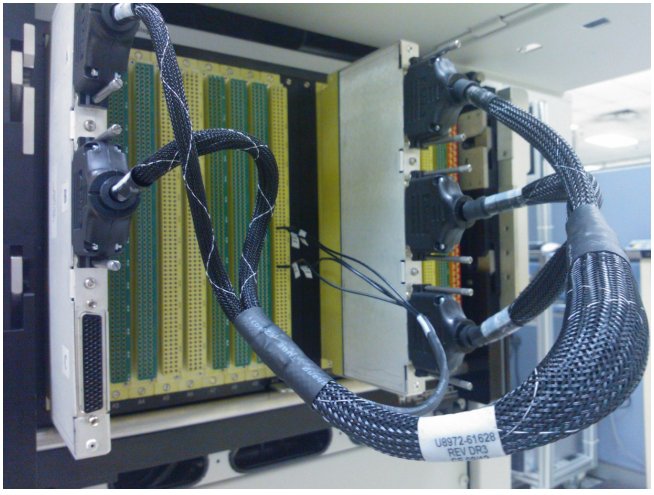


Figure 3-4 shows a Universal CEDGN Test Fixture U8972-67901 connected to Slot 1 and another Universal CEDGN Test Fixture U8972-67901 connected to Load Card Slot (13-15 and 18-20). A CEDGN Load Card Cable U8972-61628 is used to link the two Universal CEDGN Test Fixtures U8972-67901 together.

Figure 3-4 Installing two Universal CEDGN Test Fixtures U8972-67901 with a CEDGN Load Card Cable U8972-61628



The ISense pins of CEDGN Load Card Cable U8972-61628 are manually probed to Slot 10 as shown in Figure 3-5. This fixture connection is used to test the connectivity and load card functionality.

Figure 3-5 ISense Pins of CEDGN Load Card Cable U8972-61628 are manually probed to ICA Slot 10

Figure 3-6 shows a Universal CEDGN Test Fixture U8972-67901 connected to Slot 1 with a CEDGN HD Load Card Cable U8972-61629 J2 connector connected to Slot 21. The ISense pins of CEDGN HD Load Card Cable U8972-61629 are manually probed to Slot 10 as shown in Figure 3-5. This fixture connection is used to test the connectivity and HD load card functionality.

Figure 3-6 Installing a Universal CEDGN Test Fixture U8972-67901 with a CEDGN HD Load Card Cable U8972-61629

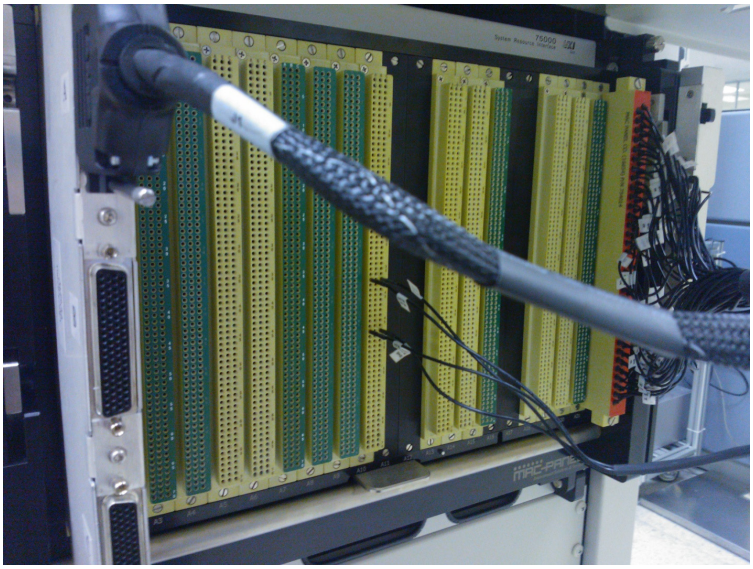
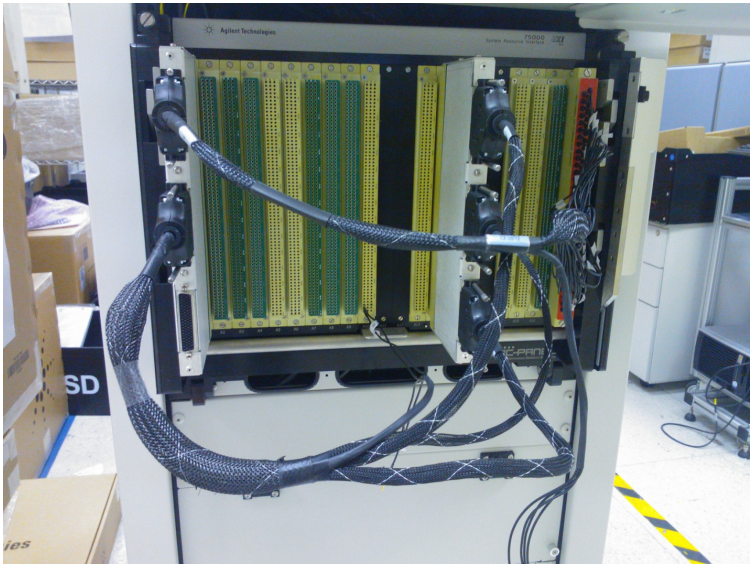


Figure 3-7 shows a Universal CEDGN Test Fixture U8972-67901 connected to Slot 1 with a CEDGN HD Load Card Cable U8972-61629 J2 connector connected to Slot 21. The second Universal CEDGN Test Fixture U8972-67901 is connected to an E-Load Control Slot (13-15 and 18-20). A CEDGN E-Load Cable U8972-61630 is used to connect this Universal CEDGN Test Fixture U8972-67901 together.

Figure 3-7 Installing two Universal CEDGN Test Fixture U8972-67901 with a CEDGN HD Load Card Cable U8972-61629 and a CEDGN E-Load Cable U8972-61630



The Power pins of the CEDGN E-Load Cable U8972-61630 are manually probed to Slot 10 as shown in Figure 3-8. This fixture connection is used to test the connectivity and the E-Load functionality.

Figure 3-8 The Power Pins of the CEDGN E-Load Cable U8972-61630 are manually probed to ICA Slot 10

Figure 3-9 shows the first Universal CEDGN Test Fixture U8972-67901 connected to Slot 1 and the second Universal CEDGN Test Fixture U8972-67901 connected to the HV-DAQ Slot. A CEDGN HV-DAQ Cable U8972-61626 is used to link the two Universal CEDGN Test Fixtures U8972-67901 together. This fixture connection is used to test the connectivity and HV-DAQ functionality.

Figure 3-9 Installing two Universal CEDGN Test Fixtures U8972-67901 with a CEDGN HV-DAQ Cable U8972-61626

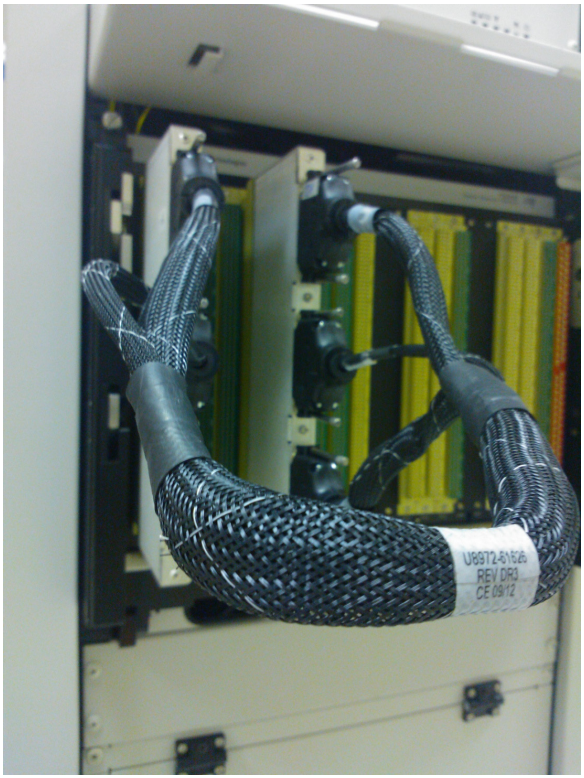
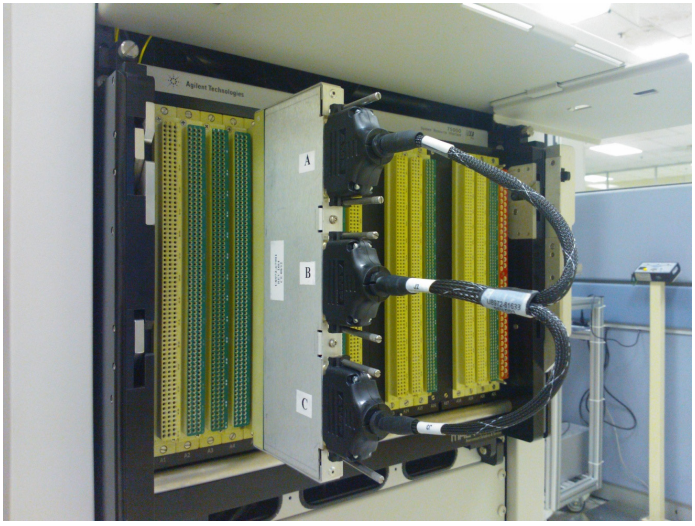


Figure 3-10 Installing the Universal CEDGN Test Fixture U8972-67901 with a CEDGN Pin Matrix Cable U8972-61633



Resolving Test Failures

Test failures can be caused by improper switch settings on the Diagnostic Test Fixture, improperly specifying the system equipment, or by an actual test system instrument failure.

Before troubleshooting the system equipment, verify that the test fixture switches are properly set and that the test system instrumentation was properly specified. If the problem seems to be the system equipment, swap the instrument and/or the cable between the instrument and the Test System Interface.

Chapter 4 contains detailed descriptions of each test that may help in isolating equipment problems to a particular component.

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4
Diagnostic Testing Details

DGN Testplan Description and Flow

The DGN testplans consist of basic tests to verify the system internal connection and basic functions of the instruments.

Section 00 Global Reset

- This section include IPC information queries, instrument initializations, and reset.

Section 01 Detecting the SLU and the First Pin Matrix

- This section first checks the presence of the SLU in the system topology file. At least one SLU must be detected to continue the test. Otherwise, the testplan will stop.
- Detecting the presence of the E8782A Instrument Matrix will follow upon a successful SLU detection. At least one instrument matrix must be present in the SLU (in the first SLU if there are two SLUs) to continue the test. Otherwise, the testplan will stop.

Section 02 Find the First DMM and Run the DMM Self-Test

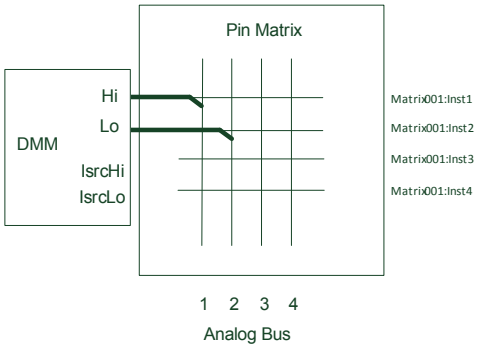
- Detects the presence of a DMM in the system topology file. At least one DMM must be present in the system to continue the test. Otherwise, the testplan will stop.
- Upon successful detection, the testplan will set all detected DMMs to run the self-test sequentially.

Section 03 Pin Matrix Non-Fixture Test with a DMM

- Sections 03 and 04 fall under the same testgroup in the testplan.
- This section consists of the pin matrix row open/close tests without fixture.

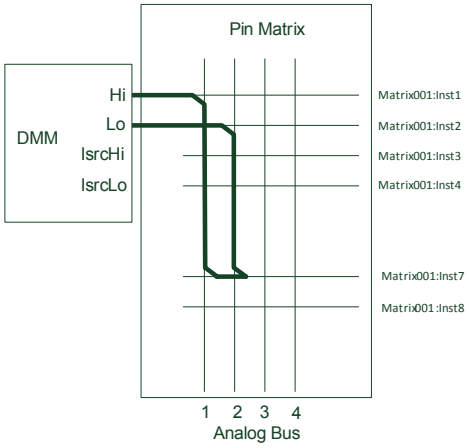
- Instrument matrix tests are as follows:
  - ABUS Short Test - Connect and measure the path resistance between DMM_Hi|ABus1 and DMM_Lo|ABus2. See Figure 4-1. There should not be any connection between the two ABUS. Repeat the test for ABus3 and ABus 4.

Figure 4-1 Measuring resistance (open) between ABus1 and ABus2 of the first pin matrix using a DMM



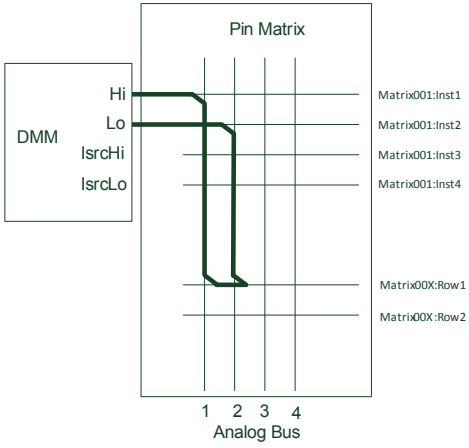
  - Instrument Rows Open/Short Test - Connect/Disconnect DMM_Hi|ABus1|Matrix001:Inst5 and DMM_Lo|ABus2|Matrix001:Inst5, and measure the path resistance. See Figure 4-2. Repeat the test for instrument rows 6 to 40. This test starts from instrument row 5 because instrument rows 1 to 4 are allocated for DMM Hi, Lo, ISrc Hi, and ISrc Lo.

Figure 4-2 Measuring resistance (close and open) between Instrument Row 7 - ABus1 and Instrument Row 7 - Abus2 relays



- Measurement Rows Open/Short Test - Connect/Disconnect DMM_Hi|ABus1|Matrix001:RowX and DMM_Lo|ABus2|Matrix001:RowX, and measure the path resistance. See Figure 4-3. Repeat the test for X = 2, 3, ..., 40.

Figure 4-3 Measuring resistance (close and open) between Row 1 - Abus 1 and Row 2 - Abus 2 relays

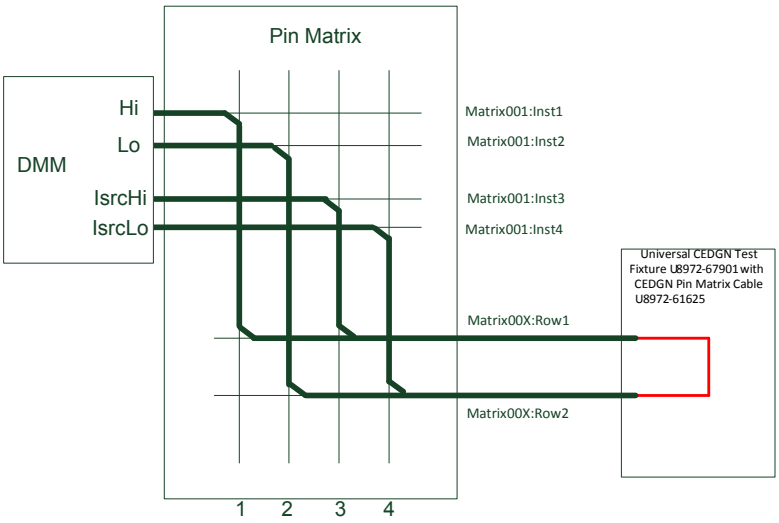


- Pin matrix tests are as follows:
  - Measurement Rows Open/Short Test - Connect/Disconnect DMM_Hi|ABus1|Matrix001:RowX and DMM_Lo|ABus2|Matrix001:RowX, and measure the path resistance. Refer to the similar connection in Figure 4-3. Repeat the test for X = 2, 3, ..., 64, and for all pin matrices present in the system.

Section 04 Pin Matrix Fixture Test with a DMM

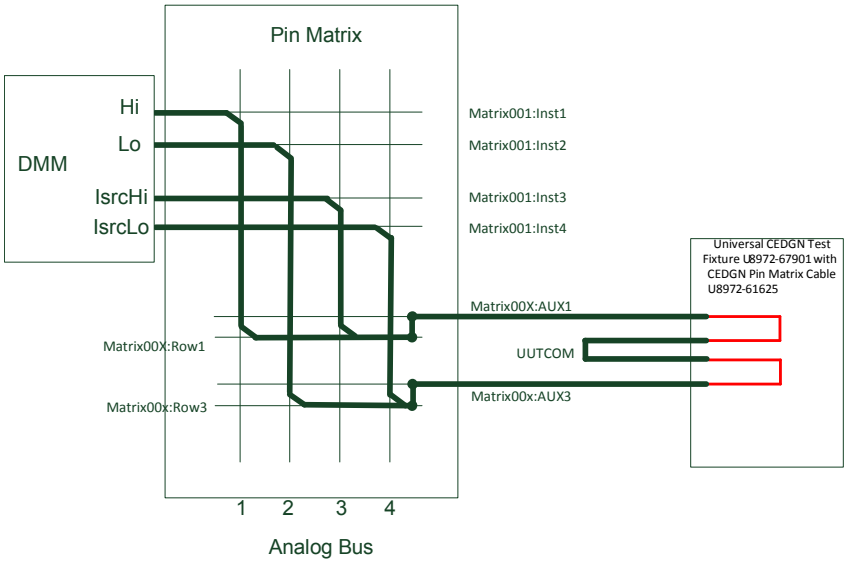
- This section requires the external fixture and loopback cable to test the relays open/short between pin matrix ROW and AUX. It is similar to the pin matrix test in the CEDGN testplan (refer to "Tests 00100: Pin Matrix Test Group"). Figure 4-3 and Figure 4-4 illustrates the internal and external connections for this test.
- Using the U8972-61625 loopback cable, pin matrix Row1 will be shorted to Row2, Row3 to Row 4, and so on until Row63 is shorted to Row64 (or Row 39 is shorted to Row40 if it is the instrument matrix). The DMM should measure SHORT when the internal switching is done. See Figure 4-4.

Figure 4-4 Measuring resistance (0 Ω) for matrix loopback row1 and row2 using DMM



- For the AUX test, the U8972-61625 loopback cable connects AUX1 to AUX 3 via the UUTCOM, similarly for AUX2 to AUX4 and so on until AUX62 is connected to AUX64 (or AUX 38 is connected to AUX40 if it is the instrument matrix). The DMM should measure SHORT when the internal switching is done. See Figure 4-5.

Figure 4-5 Measuring resistance value (0 Ω) for loopback AUX1 and AUX3 with uutcom closed test using DMM



Section 05 Check the SLU DAC Functionality

- This test measures the accuracy of the SLU DAC using a DMM.
- The SLU DAC is set to output 5 V and the DMM will measure its accuracy. Repeat the test for DAC voltage –5 V.

Section 06 Digitizer test - Auto-Detect, Self-Test, and Measure

- This test detects if one or more digitizer is present in the system and runs the self-test for each detected digitizer. The self-test returns a PASS result if the return value is zero.
- The SLU DAC (or first SLU detected if there are two SLUs) will provide the source to validate the digitizer functionality. The SLU DAC is set to output 10 V and the digitizer will measure this output voltage level.

- A connection is made between the digitizer and the SLU DAC. SLU DAC 1 will be connected to the first channel of the digitizer. SLU DAC 2 will be connected to the second channel of the digitizer. Only the first two channels of the digitizer will be tested even if the digitizer has more than two channels. SLU DAC 1 is set to output 10 V and the digitizer measures the voltage from its first or only channel followed by SLU DAC 2 output of 10 V to be measured by the second channel of the digitizer where applicable.
  - Connection for Channel 1 of Digitizer to SLU DAC 1:
    - matrix1-Inst7|ABus1|dmm:Hi|matrix1:DAC1Rly
    - matrix1-Inst8|ABus2|dmm:Lo|matrix1:EarthGnd
  - Connection for Channel 2 of Digitizer to SLU DAC 2:
    - matrix1-Inst9|ABus3|dmm:Hi|matrix1:DAC2Rly
    - matrix1-Inst10|ABus4|dmm:Lo|matrix1:EarthGnd
- Refer to Figure 4-6 for the Channel 1 connection and Figure 4-7 for the Channel 2 connection.

Figure 4-6 Measuring the SLU DAC 1 Output Voltage (+10 V) using Channel 1 of the Digitizer for digitizer functionality verification

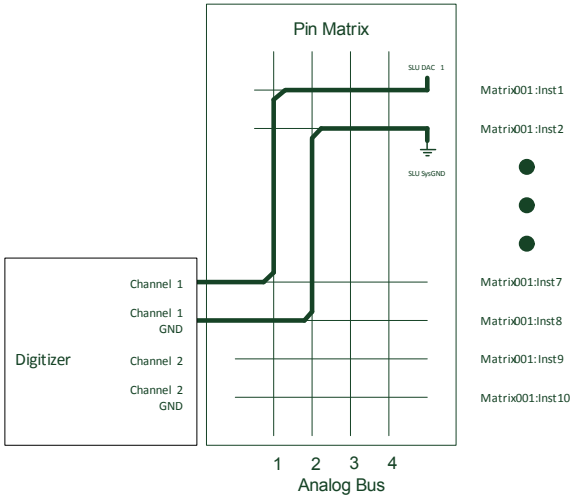
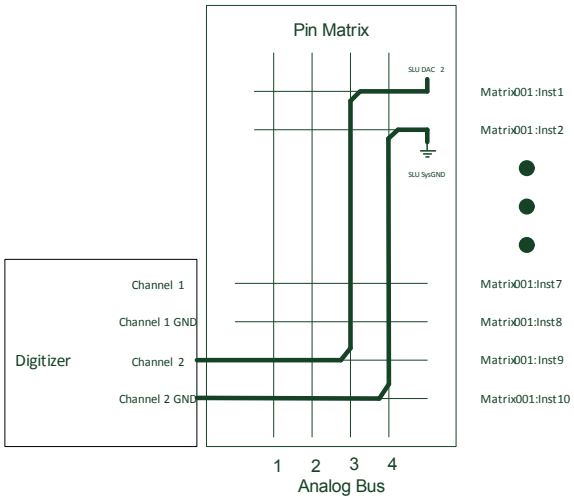


Figure 4-7 Measuring the SLU DAC 2 Output Voltage (+10 V) using Channel 2 of the Digitizer for digitizer functionality verification



Section 07 HV-DAQ Test - Auto-Detect and Read Card Information

Section 08 V/I Source Test - Auto-Detect and Read Card Information

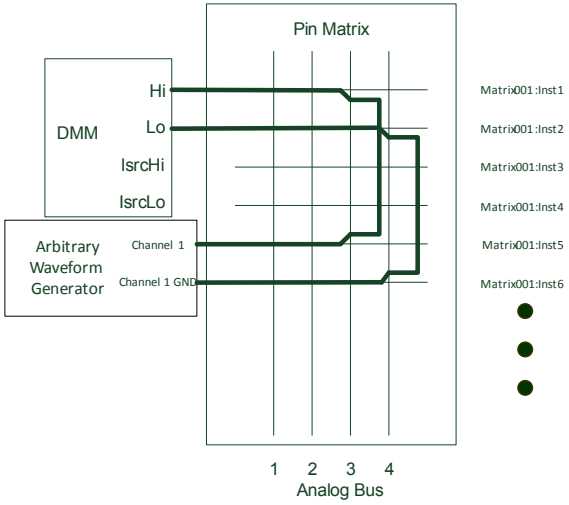
- These sections both detect if one or more HV-DAQ (or V/I source) is present in the system.
- The test queries the card information from each detected HV-DAQ (or V/I Source). The functionality test for HV-DAQ (or V/I Source) will be covered in the CEDGN test, see "Tests 01600: HV-DAQ" (or "Tests 01400: V/I M9186A").

Section 09 Arbitrary Waveform Generator (AWG) test - Auto-Detect, Read Card Info, and Measure DC Output with DMM

- This test detects if one or more AWG is present in the system.

- This test queries the card/module information for each detected AWG and runs the self-test. The self-test returns a PASS result if the return value is 0.
- The AWG is set to output 10 V DC and a DMM measures its output.
  - The AWG to DMM connection is as follows:
    - matrix1-Inst5|ABus3|matrix1-Inst1
    - matrix1-Inst6|ABus4|matrix1-Inst2
- Figure 4-8 illustrates the internal switching connection. Only Channel 1 will be tested. Testing Channel 2 requires an external fixture and will be covered in the CEDGN test, "Tests 01000: Arb 33522A" and "Tests 01100: Arb PXA722x".

Figure 4-8 Measuring the Arbitrary Waveform Generator output (+10 V) using a DMM



Section 10 DAC Test - Auto-Detect and Read Card Information

- Detects if one or more DAC is present in the system.
- This test queries the card information from each detected DAC.

- The functionality test for the DAC will be covered in the CEDGN test, see "Tests 01500: DAC M9185A".

Section 11 E-Load Mainframe Test

Section 12 Power Supply Mainframe Test

- Sections 11 and 12 detects if one or more E-load mainframe (or power supply mainframe) is present in the system and runs the self-test.
- The self-test returns a PASS result if the return value is zero.

CEDGN Testplan Description and Flow

Tests 00000: GlobalReset

- This test initializes and resets all instruments in the system topology file.

Tests 00100: Pin Matrix Test Group

Call sequence: *E8782A pin matrix test*

E8783A pin matrix test

- Each pin matrix test sequence consist of tests to verify the open/close of relays between ROW and between ROW, AUX, and UUTCOM.

  Figure 4-9 illustrates the measurement path for ROW tests. Row1 and Row2 are shorted using the U8972-67901 Universal CEDGN Test Fixture and the U8972-61625 loopback cable. The DMM is expected to measure SHORT (0 Ω).

  Figure 4-10 illustrates the measurement path for AUX tests. In this test, the U8972-61625 loopback cable connects AUX1 to AUX 3 via UUTCOM, similarly for AUX2 to AUX4 and so on until AUX62 is connected to AUX64 (or AUX 38 is connected to AUX40 if it is the instrument matrix). The DMM is expected to measure SHORT (0 Ω).

Figure 4-9 Measuring the loopback resistance value (0 Ω) between Row1 and Row2 using a DMM[1]

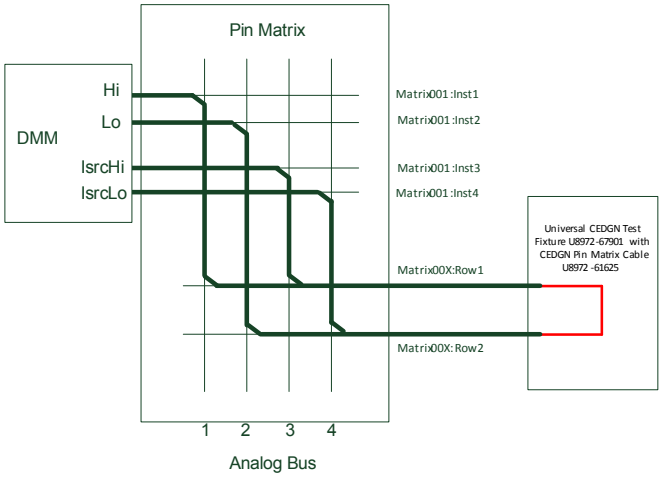
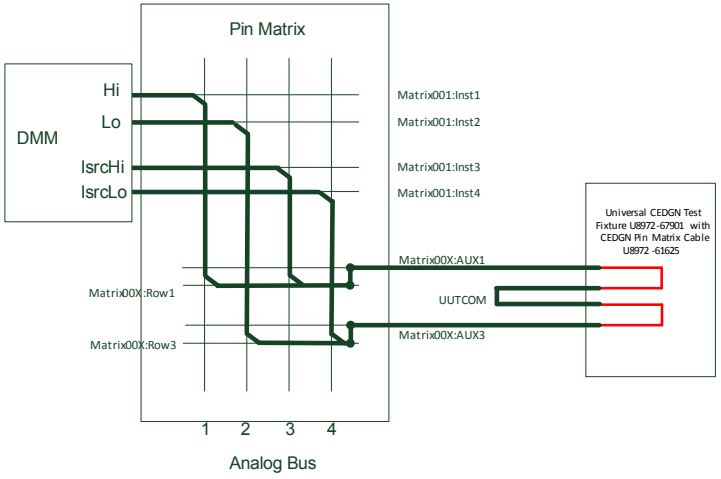


Figure 4-10 Measuring the loopback resistance value (0 Ω) between AUX1 and AUX3 via UUTCOM using a DMM[1]



[1] Where X represents the number of the specific matrix card.

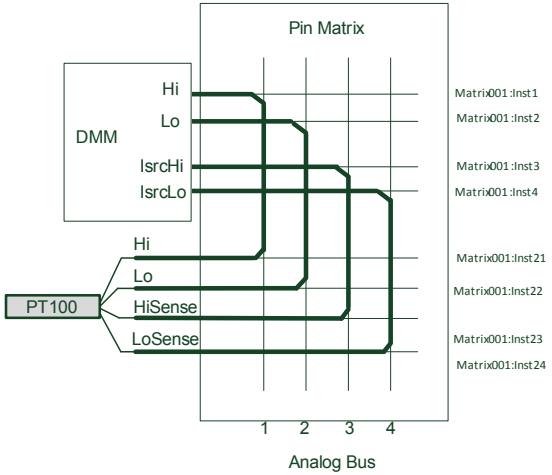
Tests 00200: ABus Debug Panel

- This section verifies the presence of physical connections between the ABus debug ports (on the ABus debug panel at system front) and connector J1 (ABus access) of the E8782A instrument matrix.
- This testplan will prompt to fix the 50 Ω load (1250-2771) on the ABus debug port under test. The DMM should measure 50 Ω.

Tests 00300: PT100 Temperature Sensor

- In a standard system, the U8972-61631 PT100 thermistor (or temperature sensor) connects to a DMM via the instrument matrix. The DMM will measure the system internal ambient temperature. See Figure 4-11.

Figure 4-11 Measuring temperature from the U8972-61631 thermistor sensor using a DMM via the instrument matrix



Tests 00400: SLU Utility Test Group

Call sequence: *1st SLU Utility test*

2nd SLU Utility test

- This test group verifies the connectivity of the SLU Inst DAC, Fixture ID, SLU Digital IO, SLU Power Buses Sense, SLU Open Drain Output, SLU System Ground, and SLU Current Sense. For the second SLU only the Current Sense and Power Buses Sense are accessible. Refer to Figure 3-3 for the CEDGN kit connection.

Tests 00500: PCI1750

Call sequence: *PCI1750*

- This test sequence verifies the presence of physical connections between the PCI 1750 DIO Card to the system ICA by writing digital data to the specified output ports, and reading back the data from the specified input ports.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

Tests 00600: COM1 and COM2

- This test group verifies the presence of physical connections between COM1 and COM2 to the system ICA through a loopback test. Specific data bytes are sent and read back from the serial port under test.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

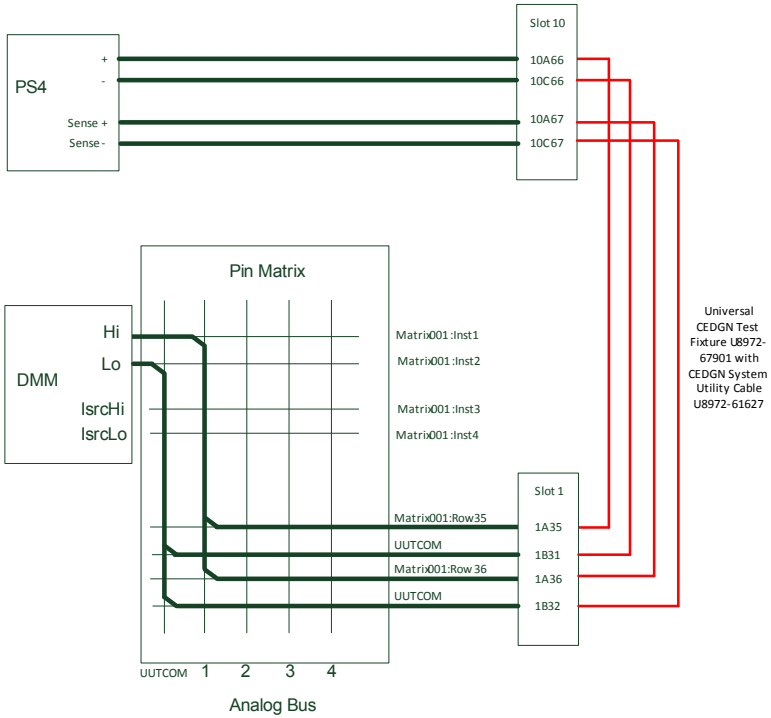
Tests 00700: Softing CAN PCI

- This test group sets up the Softing CAN-AC2-PCI card and verifies the presence of physical connections between CAN-AC2-PCI Channel 1 and Channel 2 to the system ICA through loopback test. Channel 1 will transmit a data frame that will be received by Channel 2 and vice versa.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

Tests 00800: DUT PS to MAC S75 interconnect

- The DUT Power Supply here refers to an instrument power supply such as the N670x.
- This test group verifies the presence of physical connection between the DUT PS to the system ICA. Each DUT PS is set to output 5 V and a DMM will measure the output from the respective modules.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test. Figure 4-12 below shows the connections between the PS4 and a DMM.

Figure 4-12 Measuring voltage (5 V) from PS4 using a DMM via the instrument matrix



Tests 00900: Utility Power Supply

- This test group verifies the presence of a physical connection between a +12 V and a +24 V Utility Power Supply to the system ICA by measuring the respective output with a DMM. The DMM is expected to measure +12 V and +24 V respectively.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

Tests 01000: Arb 33522A

Tests 01100: Arb PXA722x

Call sequence: *33522A test*

PXA722x test

- Both test sequence verifies the presence of a physical connection between the Arbitrary Waveform Generator (AWG), pin matrix, and system ICA.
- Figure 4-13 illustrates the internal switching connection to test AWG Channel 1. AWG Channel 1 is set to output DC +10 V and a DMM will measure its output.
- Figure 4-14 illustrates the internal and external switching connections to test AWG Channel 2. AWG Channel 2 is set to output DC +10 V and a DMM will measure its output.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

Figure 4-13 Measuring DC +10 V generated from the Arbitrary Waveform Generator Channel 1 using a DMM via the instrument matrix

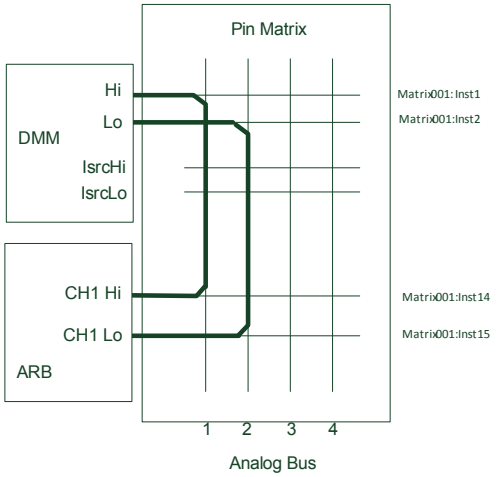
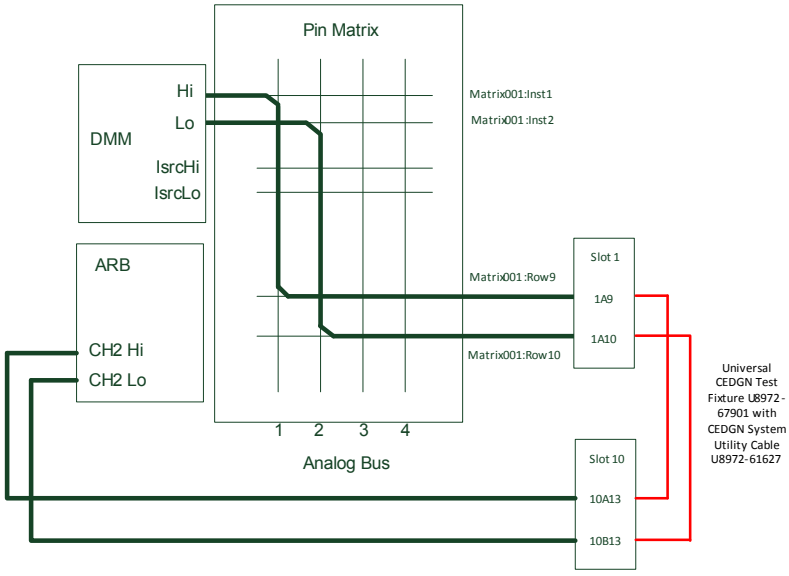


Figure 4-14 Measuring DC +10 V generated from the Arbitrary Waveform Generator Channel 2 using a DMM via the instrument matrix and the System ICA



Tests 01200: ADC L453xA

Tests 01300: ADC PXD7314

Call sequence: *L453xA test*

PXD7314 test

- Both test sequence verifies the presence of a physical connection between the L453x digitizer (or PXD7314), pin matrix, and system ICA.
- Figure 4-15 illustrates the internal switching connection to test digitizer Channel 1. Similar connections apply for Channel 2. In this test, the SLU DAC1 is set to output +10 V and the digitizer will measure the voltage.
- Figure 4-16 illustrates the internal and external switching connections to test digitizer Channel 3. Similar connections apply for Channel 4. The SLU DAC1 is set to output +10 V and the digitizer will measure the voltage.
- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

Figure 4-15 Measuring DC +10 V generated from SLU DAC1 using Digitizer Channel 1 via the instrument matrix

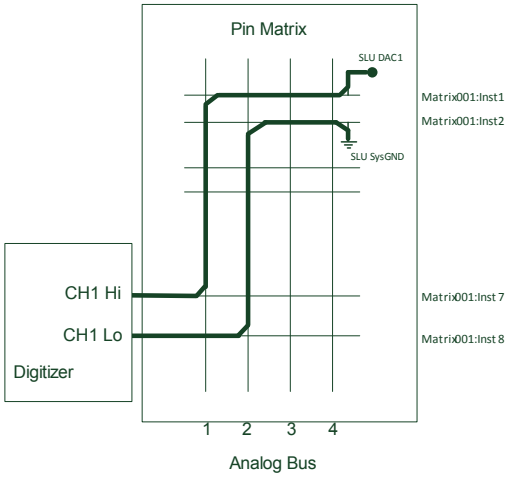
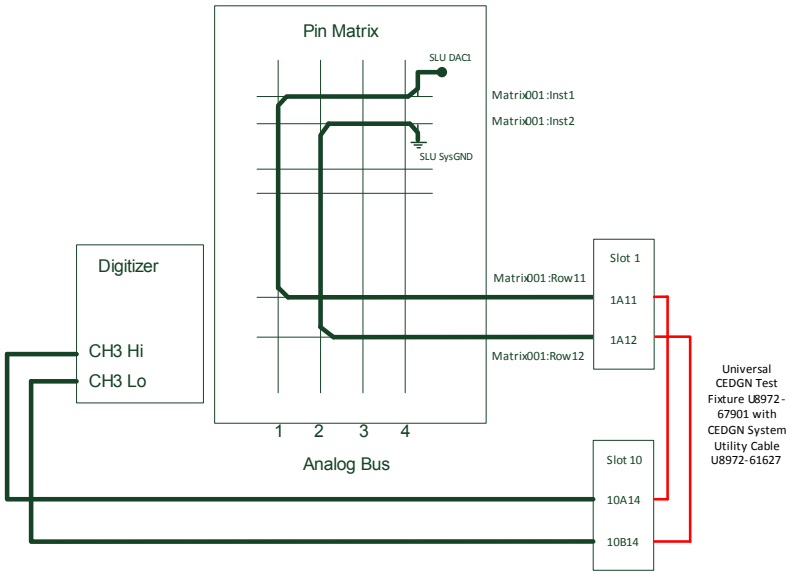


Figure 4-16 Measuring DC +10V generated from SLU DAC1 using Digitizer Channel 2 via the instrument matrix and the System ICA



Tests 01400: V/I M9186A

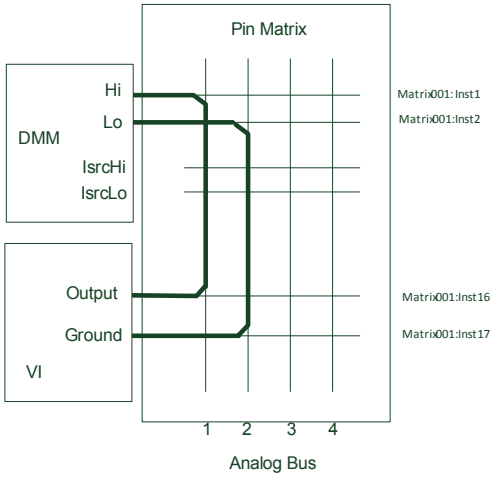
Call sequence: *VI M9186A test*

- This test sequence verifies the presence of a physical connection between the M9186A V/I Source to the instrument matrix. Table 4-1 shows the output value of the V/I source-under-test in voltage or current mode, low or high range. Figure 4-17 illustrates the internal switching connection for the DMM to measure the voltage and current output from the V/I source-under-test.

Table 4-1 V/I Source output value

V/I Source under test	Output 1	Output 2
Low Voltage:		
0 Ω path	–16 V	16 V
10 Ω path	–16 V	16 V
100 Ω Path	–16 V	16 V
1 kΩ Path	–16 V	16 V
10 kΩ Path	–16 V	16 V
High Voltage:		
0 Ω Path	–10 V	100 V
100 Ω Path	–10 V	100 V
Low Current	–0.02 A	0.02 A
High Current	–0.2 A	0.2 A

Figure 4-17 Measuring voltage and current generated from the M9186A V/I using a DMM via the instrument matrix



Tests 01500: DAC M9185A

Call sequence: *DAC M9185A test*

- This test sequence verifies the presence of a physical connection between the M9185A DAC to the E8783A pin matrix Aux Connector and to the system ICA.
- Figure 4-18 illustrates the internal switching connection to test DAC Channel 1. Each DAC channel is set to output voltage (–16 V, +16 V, and 0 V) and a DMM will measure the respective channel under test. Note that the DAC sense lines are not connected at this stage. The same test is repeated with the DAC sense lines connected, see Figure 4-19.
- Finally, the DAC trigger function is checked with the SLU DAC1 as the trigger source. The DAC output should only be present upon trigger from the SLU DAC1. See Figure 4-20.

- This test requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61627 CEDGN System Utility Cable. See Figure 3-3 on how to connect the CEDGN kits for this test.

Figure 4-18 Measuring voltage (without sense) generated from the M9185A DAC using a DMM via the instrument matrix and pin matrix

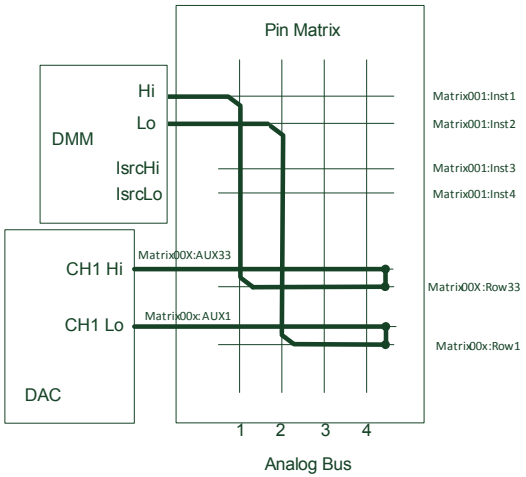


Figure 4-19 Measuring voltage (with sense) generated from the M9185A DAC using a DMM via the instrument matrix and pin matrix

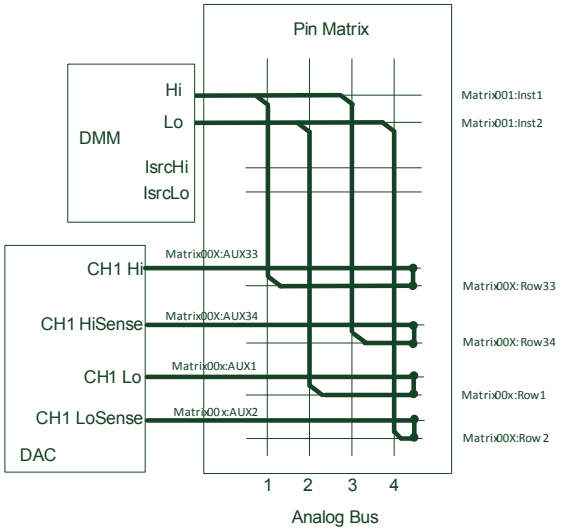
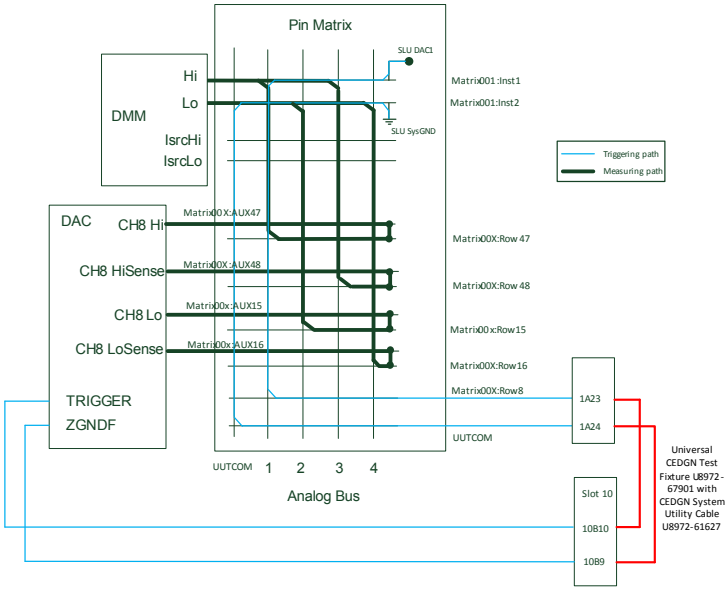


Figure 4-20 DAC output voltage upon triggered by DC voltage from SLU DAC1



Tests 01600: HV-DAQ

Call sequence: *HV-DAQ M9216A test*

- This test sequence verifies the presence of physical connection between the M9216A HV-DAQ and system ICA.
- Similar to "Tests 01200: ADC L453xA" and "Tests 01300: ADC PXD7314" for digitizers, the SLU DAC1 is set to output voltage and the HV-DAQ will measure the voltage. Figure 4-21 illustrates the internal and external switching connections to test the HV-DAQ basic functions.
- The CEDGN test kit provides the loopback between the HV-DAQ and its respective AUX. A DMM is expected to measure SHORT (0 Ω) when the necessary internal switching is done. See Figure 4-22.
- Both tests require two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61626 CEDGN HV-DAQ Cable. See Figure 3-9 on how to connect the CEDGN kits for this test.

Figure 4-21 Measuring DC Voltage generated from the SLU DAC1 using the HV-DAQ Port via the instrument matrix

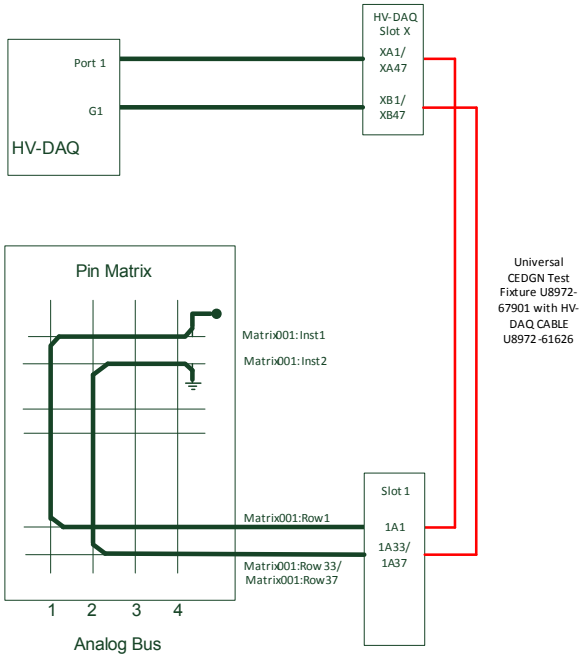
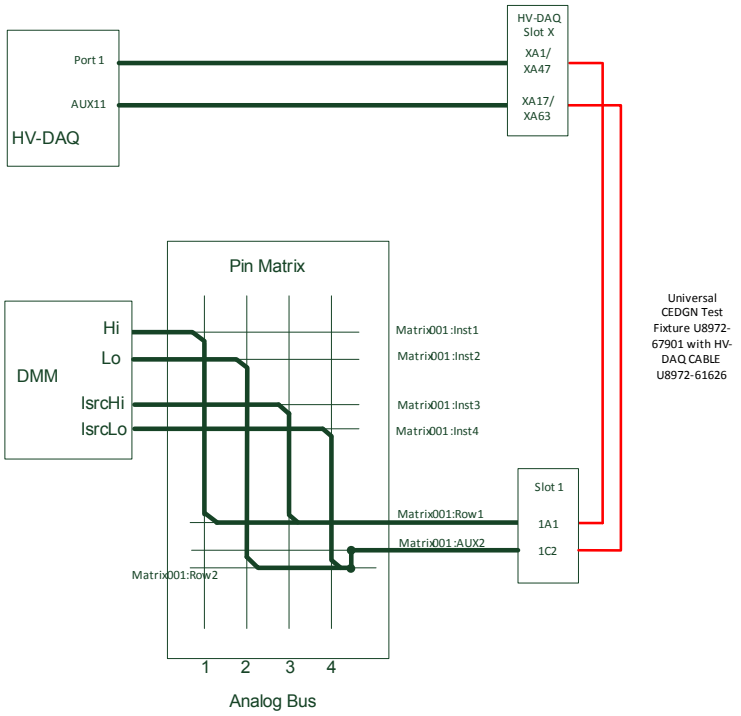


Figure 4-22 Measure loopback resistance value (0 Ω) between the HV-DAQ AUX and Port using a DMM via the instrument matrix



Tests 01700: Load Card Test Group

Call sequence: *E6175A Load Card test*

- This test sequence verifies the presence of a physical connection between the E6175A Load Card, power supply, and system ICA.
- This test sequence consists of an unpowered load card test, a powered load card test, and a current sense test.

- Load relay switches are tested in the unpowered load card test. In this test, external mount load with effective load resistance 28.86 Ω (E2240-67012) is mounted on the E6175A J1 connector. Use a DMM to measure the resistance path between channel 1 and channel 2, similarly between channel 3 and channel 4, and so on until channel 7 and channel 8. Figure 4-23 illustrates the resistance measurement path for the E6175A unpowered load card test.
- The powered load card test requires the DUT power supply. If no DUT Power Supply is present, this test will be skipped. The DUT Power Supply is set to output +5 V (current limit at 0.1 A) and a DMM will measure the voltage via load card channel, NC, and NO. Figure 4-24 illustrates the measurement path for the E6175A powered load card test.
- Figure 4-25 illustrates the internal and external switching connections to test E6175A current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-23 E6175A unpowered load card test

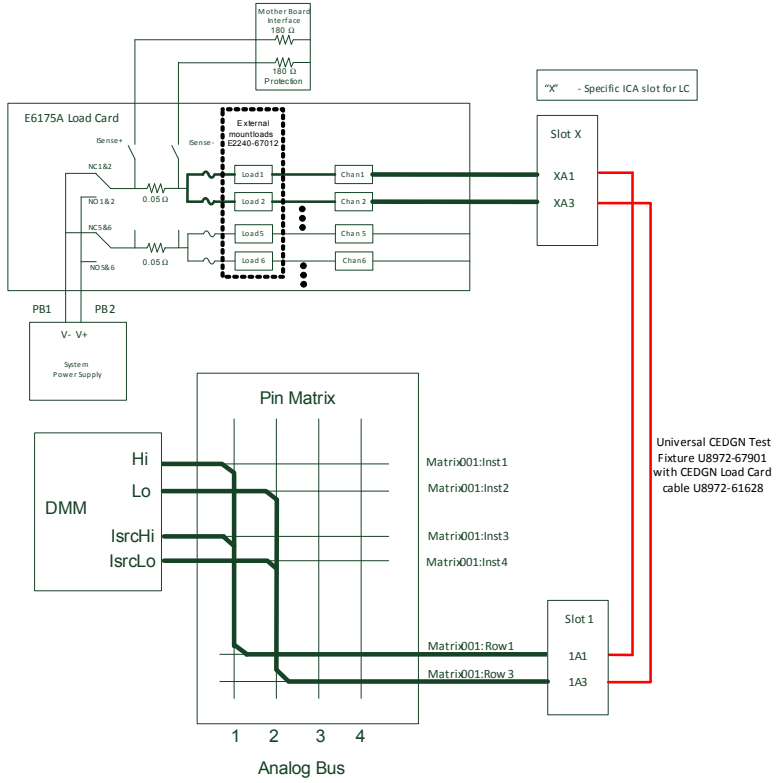


Figure 4-24 E6175A powered load card test

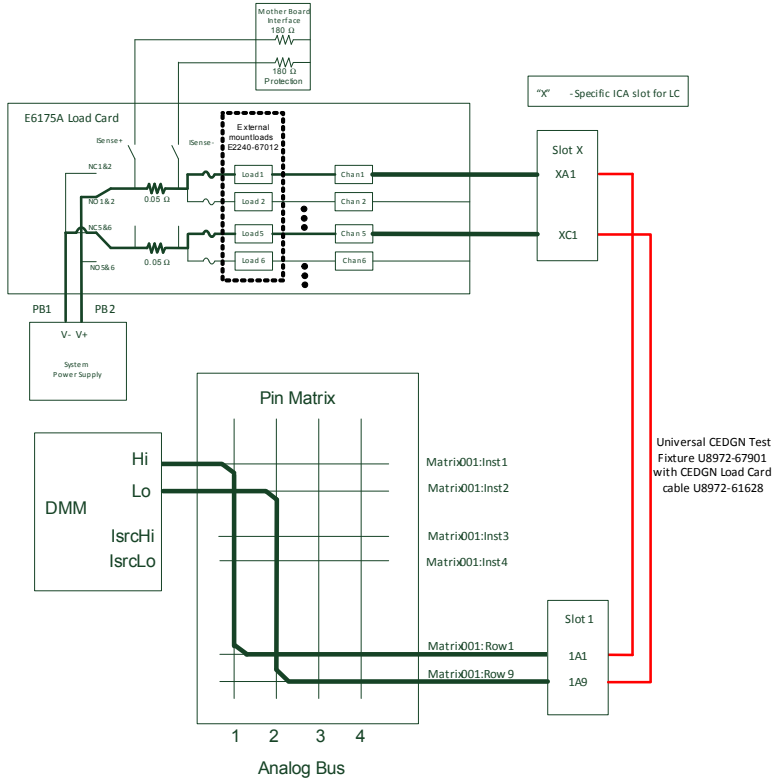
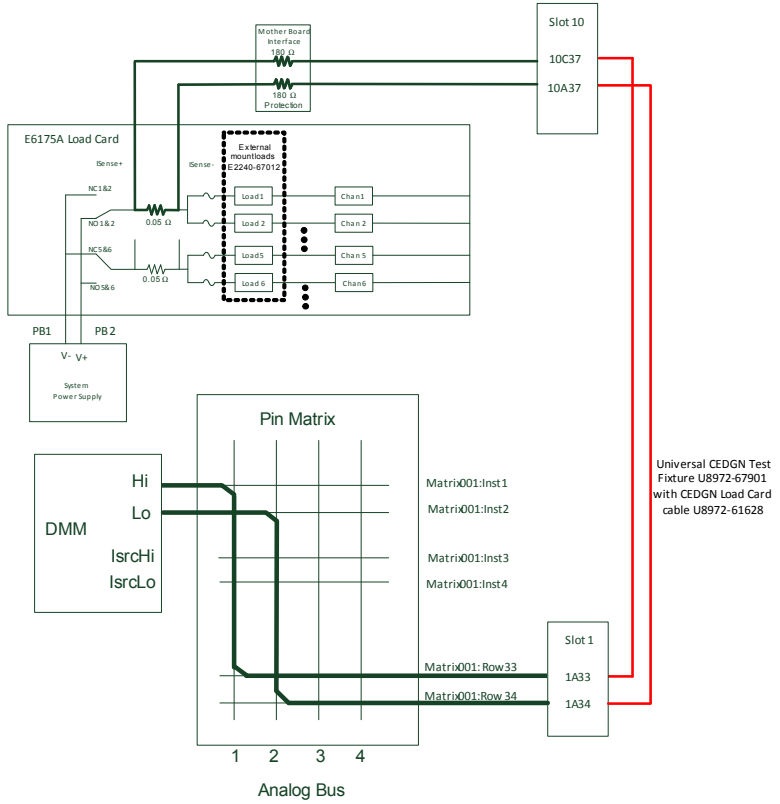


Figure 4-25 E6175A current sense test



Call sequence: *E6176A Load Card test*

- This test sequence verifies the presence of physical connection between E6176A Load Card, power supply, and system ICA.
- This test sequence consists of unpowered load card test, powered load card test, and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, external mount load with effective load resistance 28.86 Ω (E2240-67012) is mounted on E6176A J1 and J2 connector. Use DMM to measure resistance path between channel 1 and channel 9 via NC and NO, similarly for channel 2 and channel 10, and so on until channel 8 and channel 16. Figure 4-26 illustrates the resistance measurement path for E6176A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, NC and NO. Figure 4-27 illustrates the measurement path for E6176A powered load card test.
- Figure 4-28 illustrates the internal and external switching connections to test E6176A current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-26 E6176A unpowered load card test

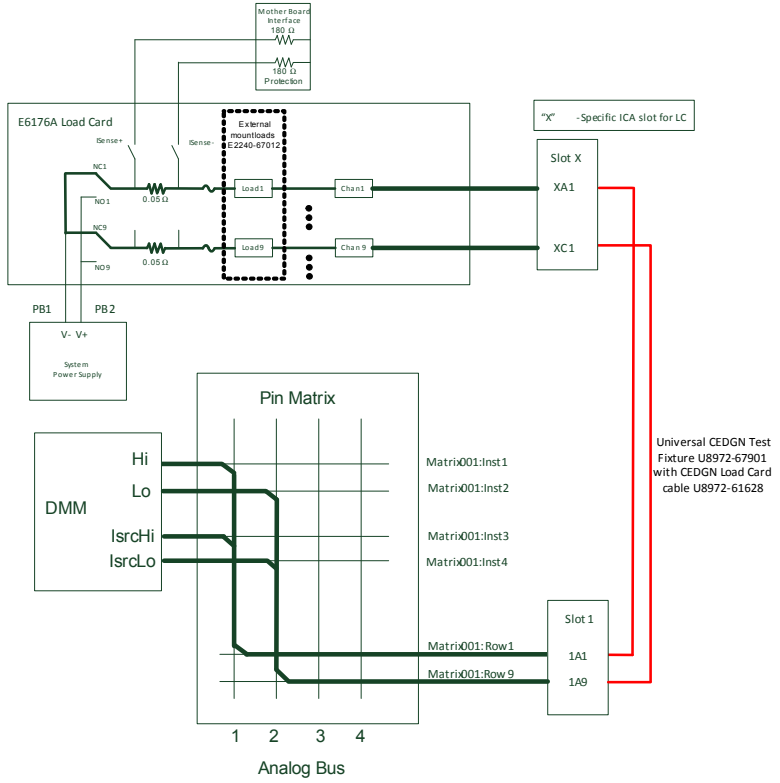


Figure 4-27 E6176A powered load card test

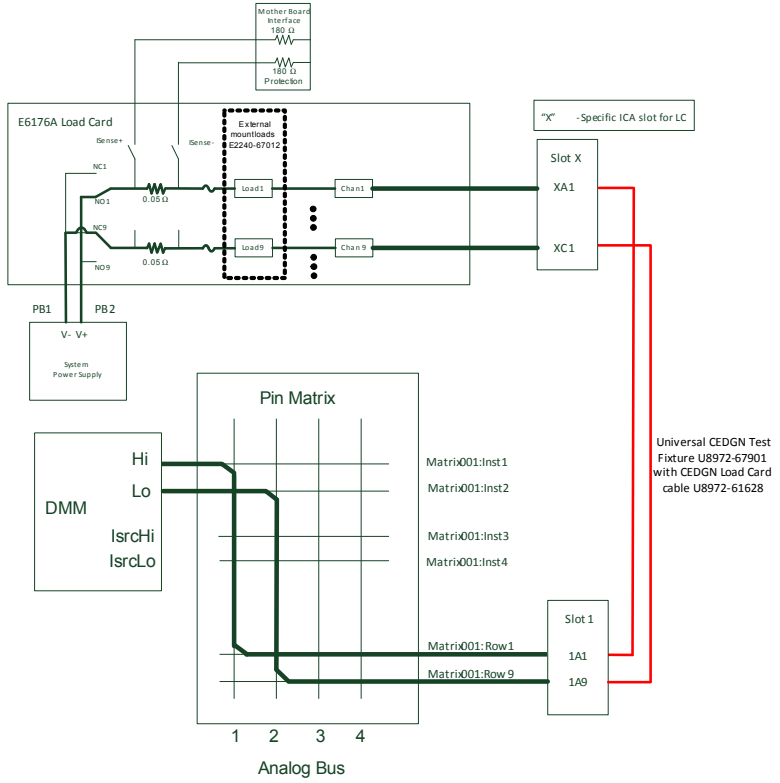
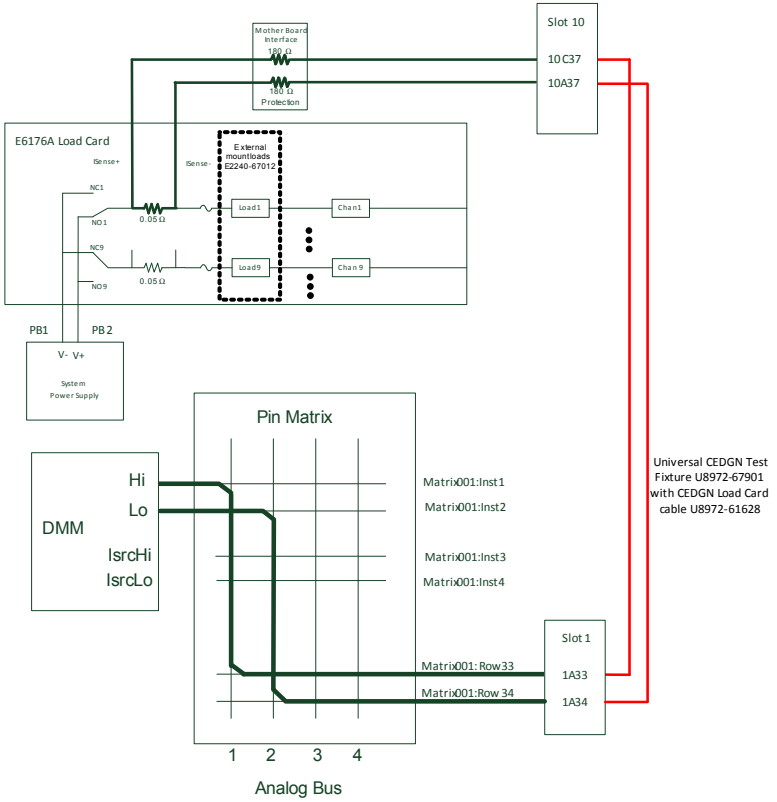


Figure 4-28 E6176A current sense test



Call sequence: *E6177A Load Card test*

- This test sequence verifies the presence of physical connection between E6177A Load Card, power supply, and system ICA.
- This test sequence consists of unpowered load card test and powered load card test.

- Load relay switches are tested in unpowered load card test. In this test, external mount load with effective load resistance 86.6 Ω (E2240-67012) is mounted on E6177A J1 connector. Use DMM to measure resistance path between channel 1 and common 1 (or channel power 1), similarly for between channel 2 and common 2, so on until between channel 24 and common 24. Figure 4-29 illustrates the resistance measurement path for E6177A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, NC and NO. Figure 4-30 illustrates the measurement path for E6177A powered load card test.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-29 E6177A unpowered load card test

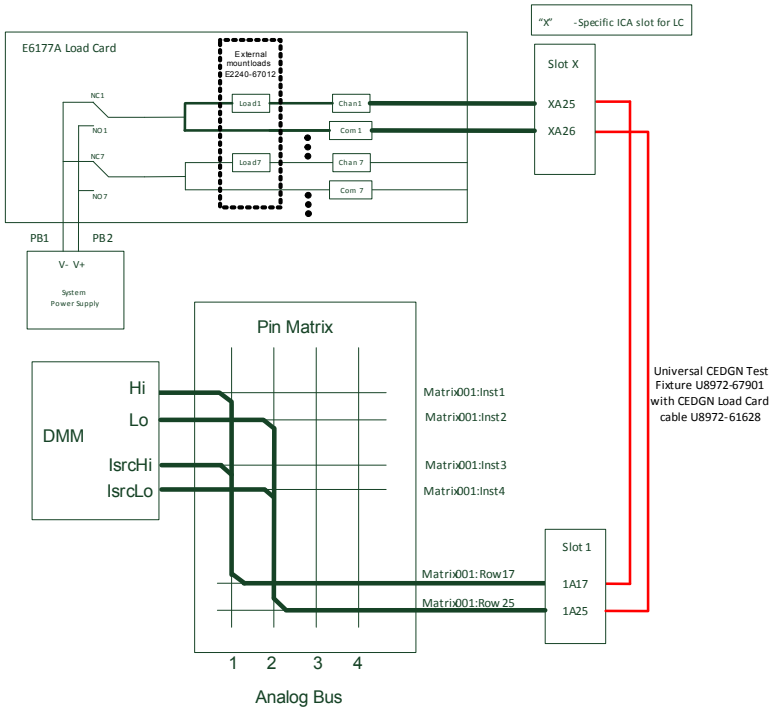
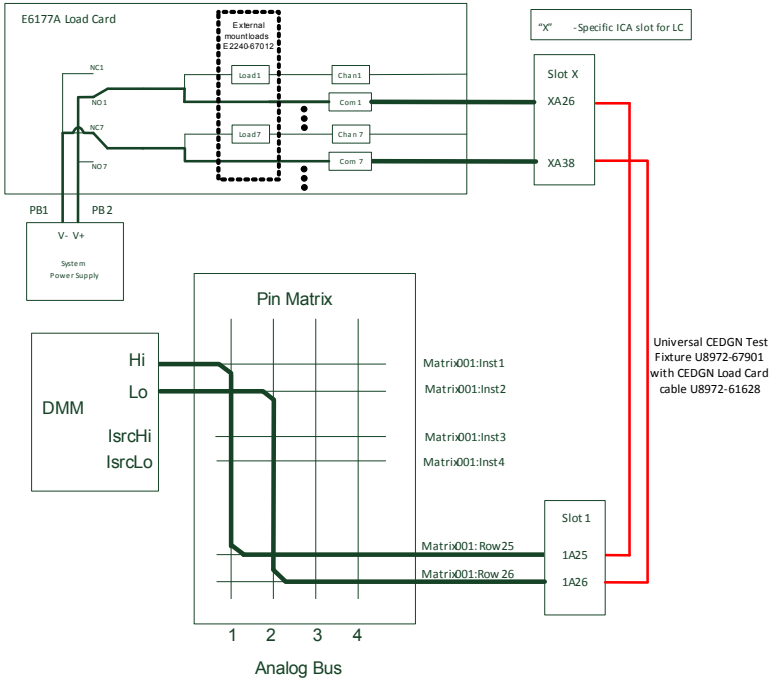


Figure 4-30 E6177A powered load card test



Call sequence: *E6178B Load Card test*

- This test sequence verifies the presence of physical connection between E6178B Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test, powered load card test and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, a loopback cable E6170-61619 is installed from E6178B J1 connector to J3 connector. Use DMM to measure resistance (0 Ω) path between channel 8 and channel 2 until channel 7. Channel 1 is not tested in this test but will test in powered load card test. Figure 4-31 illustrates the resistance measurement path for E6178B unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, P100 and P200. Figure 4-32 illustrates the measurement path for E6178B powered load card test.
- Figure 4-33 illustrates the internal and external switching connections to test E6178B current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61629 CEDGN HD Load Card Cable. See Figure 3-6 on how to connect the CEDGN kits for this test.

Figure 4-31 E6178B unpowered load card test

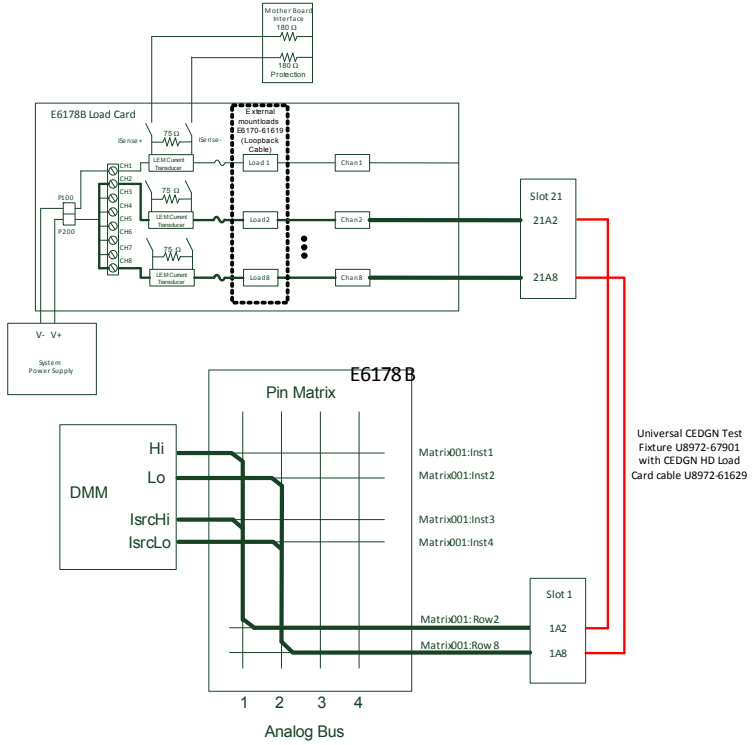


Figure 4-32 E6178B powered load card test

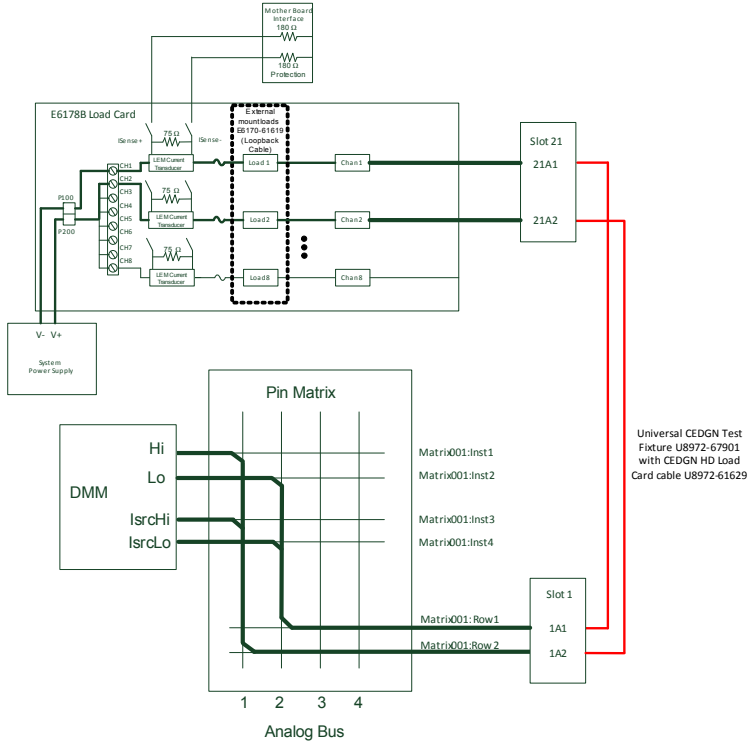
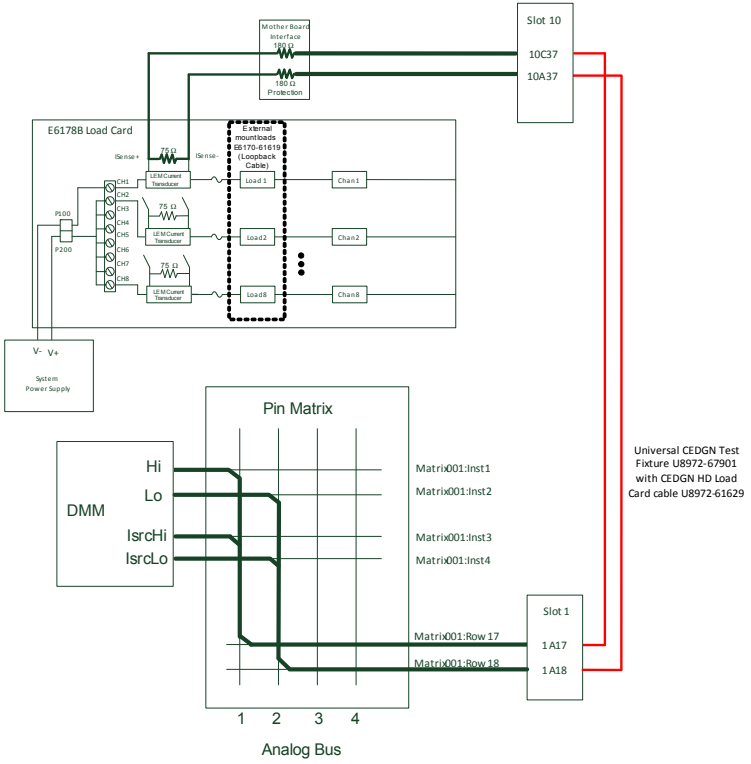


Figure 4-33 E6178B current sense test



Call sequence: *N9377A Load Card test*

- This test sequence verifies the presence of physical connection between N9377A Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test, powered load card test, and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, external mount load E2240-67012 is mounted on N9377A J1 and J2 connector. The effective load resistance on load X.1 is 28.86 Ω and on load X.2 is short (0 Ω). X represents the channel number from 1 to 16. Use DMM to measure resistance path between channel 1 and channel 9 via load1.1 and NC. The expected reading is 60.6588 Ω. Next, measure short (0 Ω) between channel 1 and channel via load1.2 and NO. This test is repeated until channel 8 and channel 16. Figure 4-34 illustrates the resistance measurement path for N9377A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, NC and NO. Figure 4-35 illustrates the measurement path for N9377A powered load card test.
- Figure 4-36 illustrates the internal and external switching connections to test N9377A current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-34 N9377A unpowered load card test

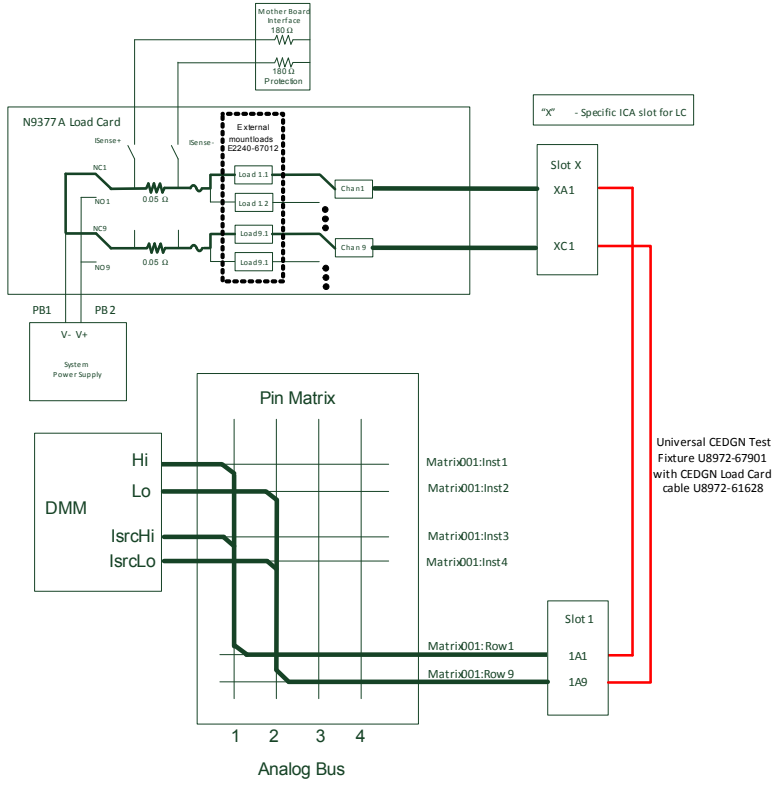


Figure 4-35 N9377A powered load card test

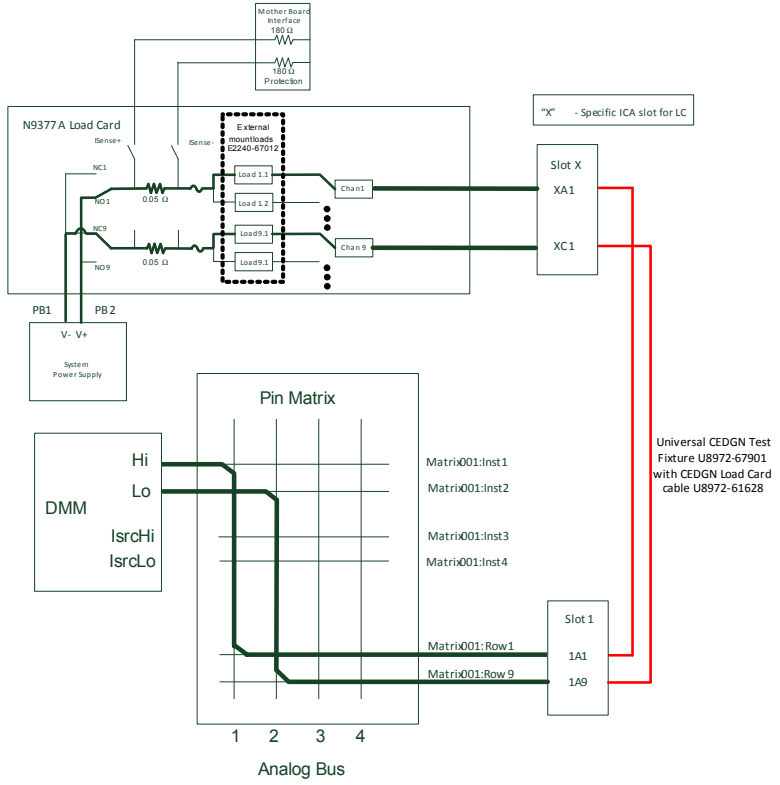
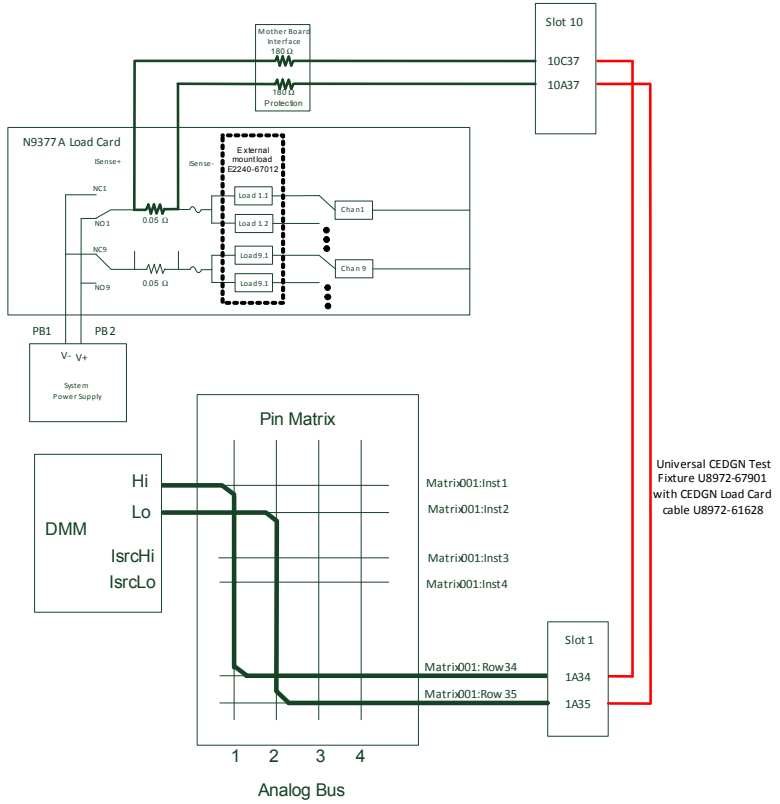


Figure 4-36 N9377A current sense test



Call sequence: *N9378A Load Card test*

- This test sequence verifies the presence of physical connection between N9378A Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test, powered load card test, and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, external mount loads with effective load resistance 820 Ω (E6170-66520) are mounted on N9378A. Use DMM to measure resistance path between channel 1 and Pwr 1 via Load1.1. This test is repeated until channel 24 with loadX.1, loadX.2, loadX.3 and loadX.4. X represents the channel number from 1 to 24. Figure 4-37 illustrates the resistance measurement path for N9378A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. There are 4 power groups for this test, Pwr 1-6, Pwr 7-12, Pwr 13-18 and Pwr 19-24. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card Power groups, NC and NO. For example, Pwr1-6 connects to NC while Pwr7-12 connects to NO and DMM measures the voltage. Test then repeats with Pwr1-6 connects to NO and Pwr7-12 connects to NC. This sequence is repeated until all load channels are tested. Figure 4-38 illustrates the measurement path for N9378A powered load card test.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-37 N9378A unpowered load card test

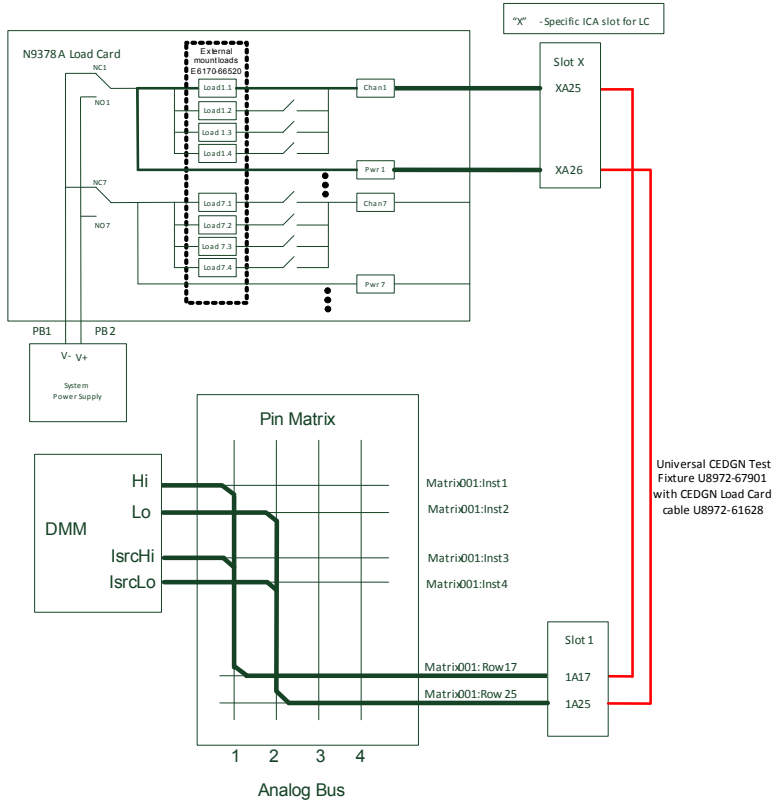
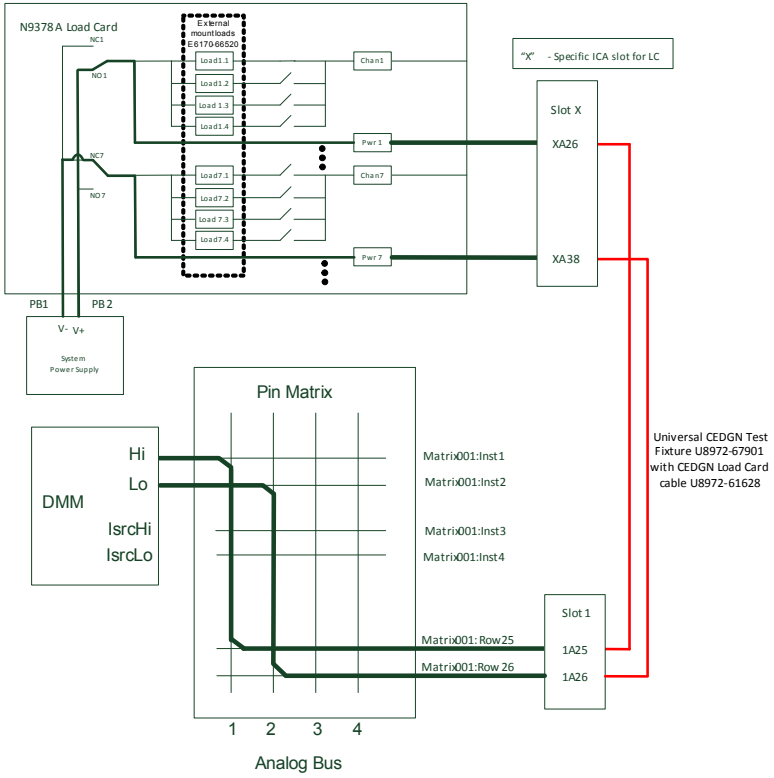


Figure 4-38 N9378A powered load card test



Call sequence: *N9379A Load Card test*

- This test sequence verifies the presence of physical connection between N9379A Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test, powered load card test, and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, external mount loads with effective load resistance 820 Ω (E6170-66520) are mounted on N9379A. Use DMM to measure resistance path between channel X and com X via loadX.1 follow by loadX.2. X represents the channel number from 1 to 48. Figure 4-39 illustrates the resistance measurement path for N9379A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. Similar toN9378A Load Card test, there are 8 power groups for this test, Pwr 1-6, Pwr 7-12, Pwr 13-18, Pwr 19-24, Pwr 25-30, Pwr 31-36, Pwr 37-42 and Pwr 43-48. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card Power groups, NC and NO. For example, Pwr1-6 connects to NC while Pwr7-12 connects to NO and DMM measures the voltage. Test then repeats with Pwr1-6 connects to NO and Pwr7-12 connects to NC. This sequence is repeated until all load channels are tested. Figure 4-40 illustrates the measurement path for N9379A powered load card test.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-39 N9379A unpowered load card test

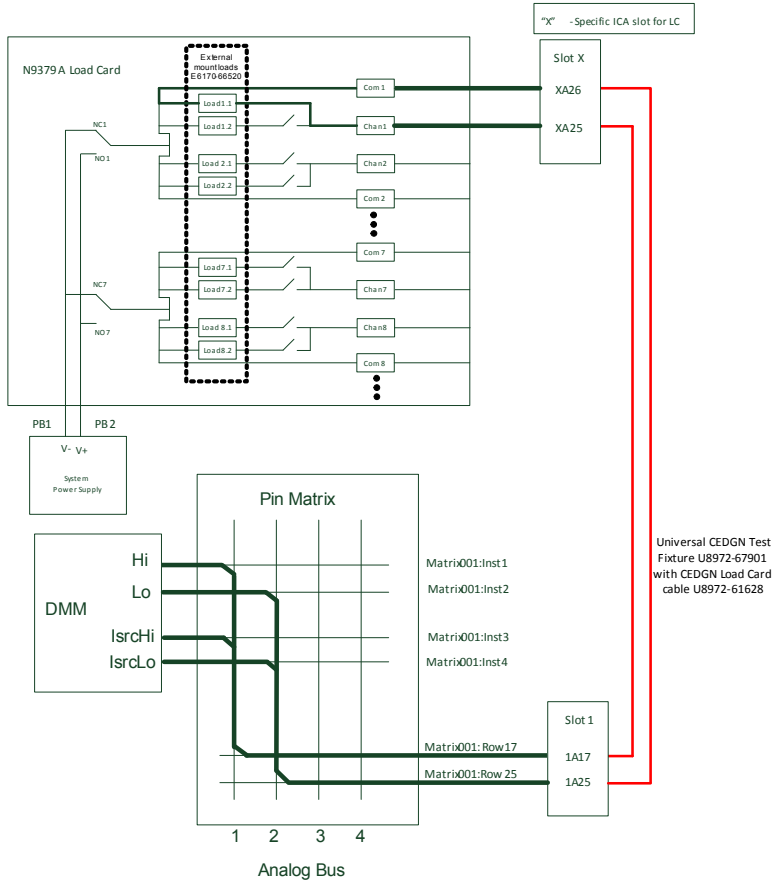
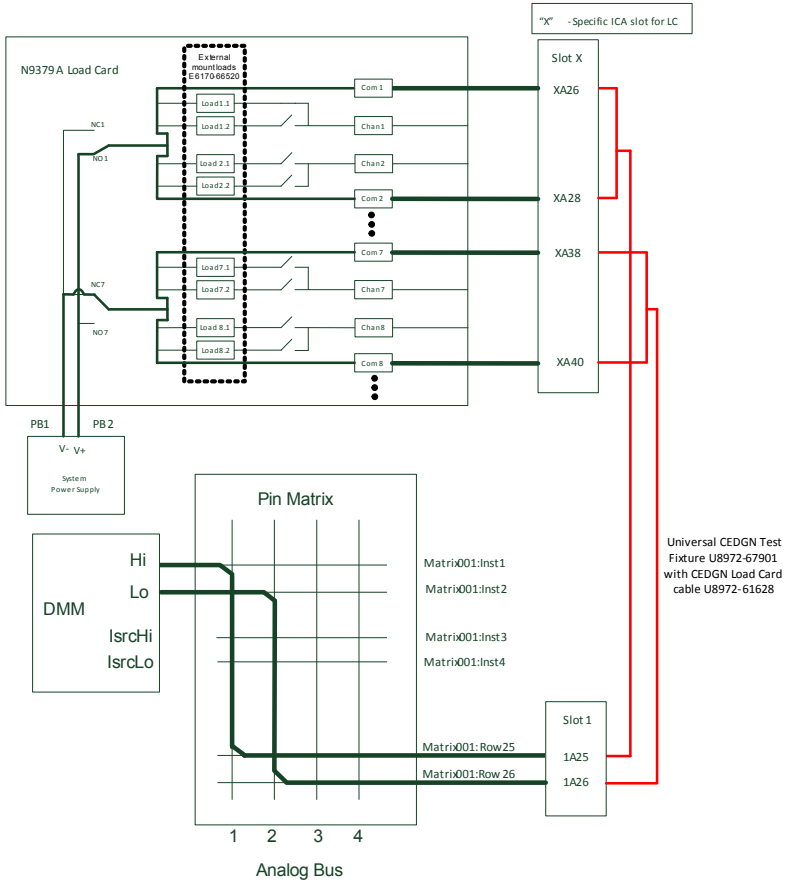


Figure 4-40 N9379A powered load card test



Call sequence: *U7177A Load Card test*

- This test sequence verifies the presence of physical connection between U7177A Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test and powered load card test.

- Load relay switches are tested in unpowered load card test. In this test, external mount load with effective load resistance 86.6 Ω (E2240-67012) is mounted on U7177A J1 connector. Use DMM to measure resistance path between channel 1 and common 1, similarly between channel 2 and common 2 and so on until between channel 24 and common 24. Figure 4-41 illustrates the resistance measurement path for U7177A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, NC and NO. Figure 4-42 illustrates the measurement path for U7177A powered load card test.
- Figure 4-43 illustrates the internal and external switching connections to test U7177A current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

Figure 4-41 U7177A unpowered load card test

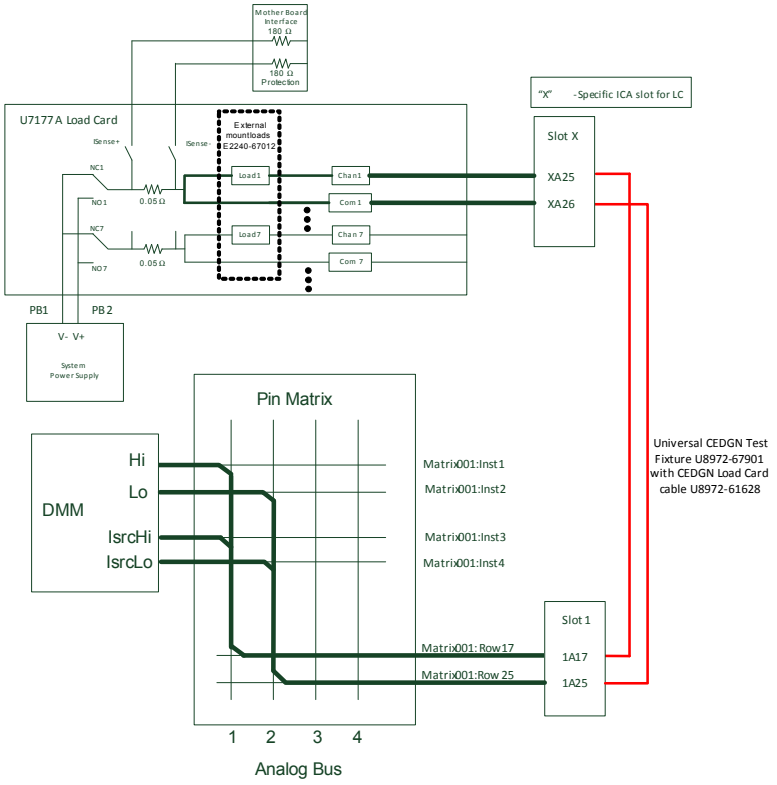
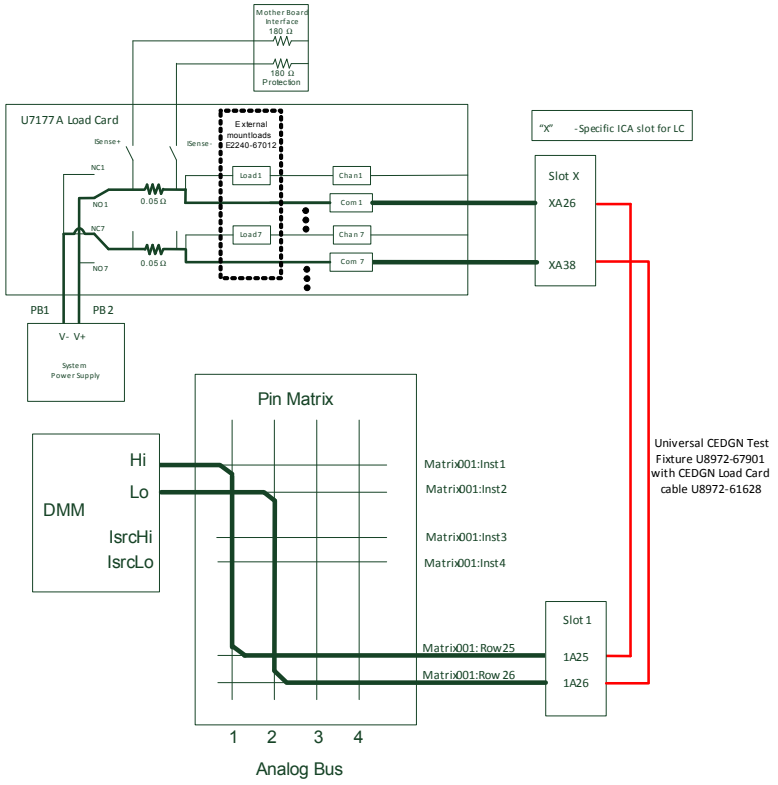


Figure 4-42 U7177A powered load card test



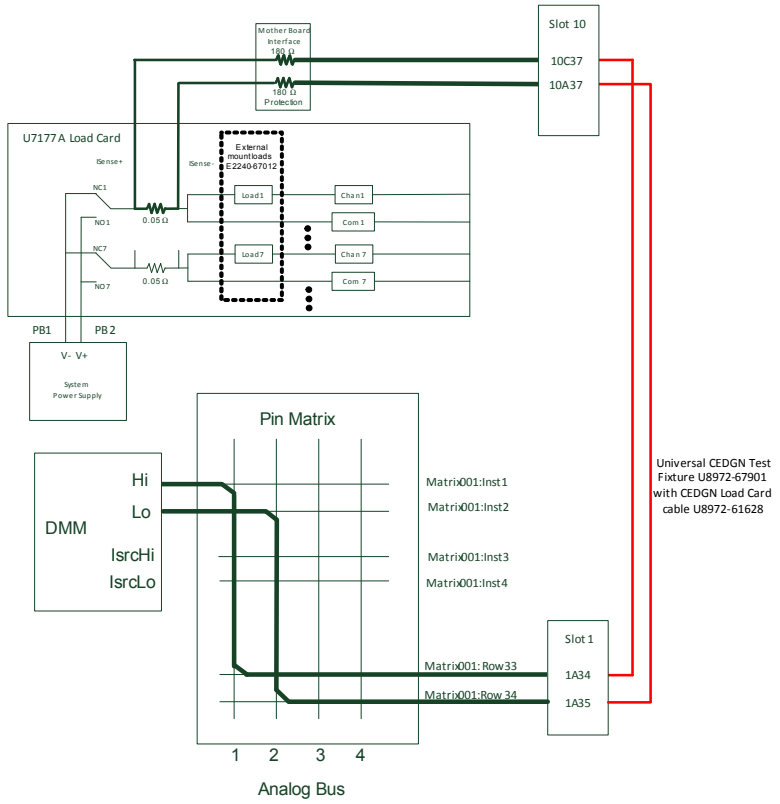


Figure 4-43 U7177A current sense test

Call sequence: *U7178A Load Card test*

- This test sequence verifies the presence of physical connection between U7178A Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test, powered load card test and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, a loopback cable E6170-61619 is installed from U7178A J1 connector to J3 connector. Use DMM to measure resistance (0 Ω) path between channel 8 and channel 2 until channel 7. Channel 1 is not tested in this test but will test in powered load card test. Figure 4-44 illustrates the resistance measurement path for U7178A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, P100 and P200. Figure 4-45 illustrates the measurement path for U7178A powered load card test.
- Figure 4-46 illustrates the internal and external switching connections to test U7178A current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 Universal CEDGN Test Fixture and a U8972-61629 CEDGN HD Load Card Cable. See Figure 3-6 on how to connect the CEDGN kits for this test.

Figure 4-44 U7178A unpowered load card test

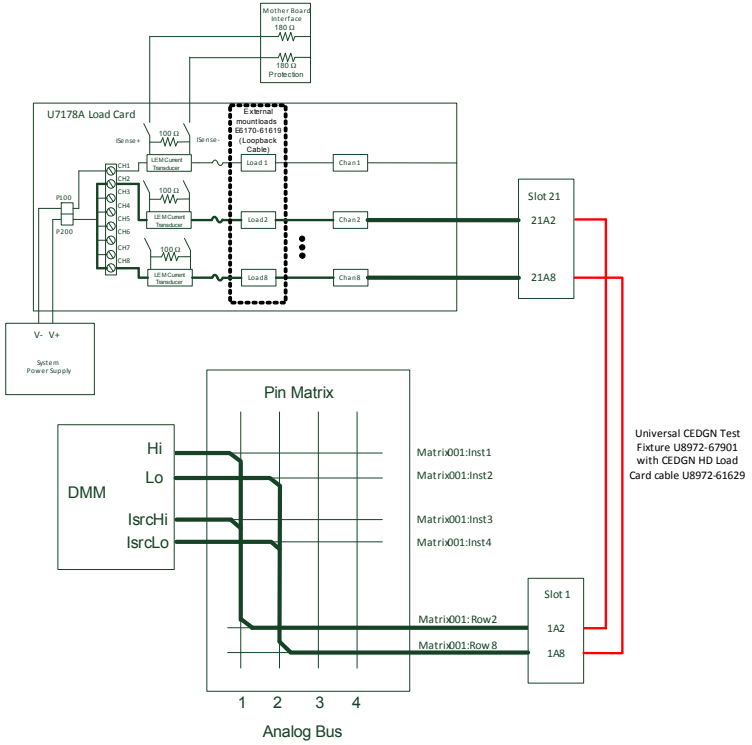


Figure 4-45 U7178A powered load card test

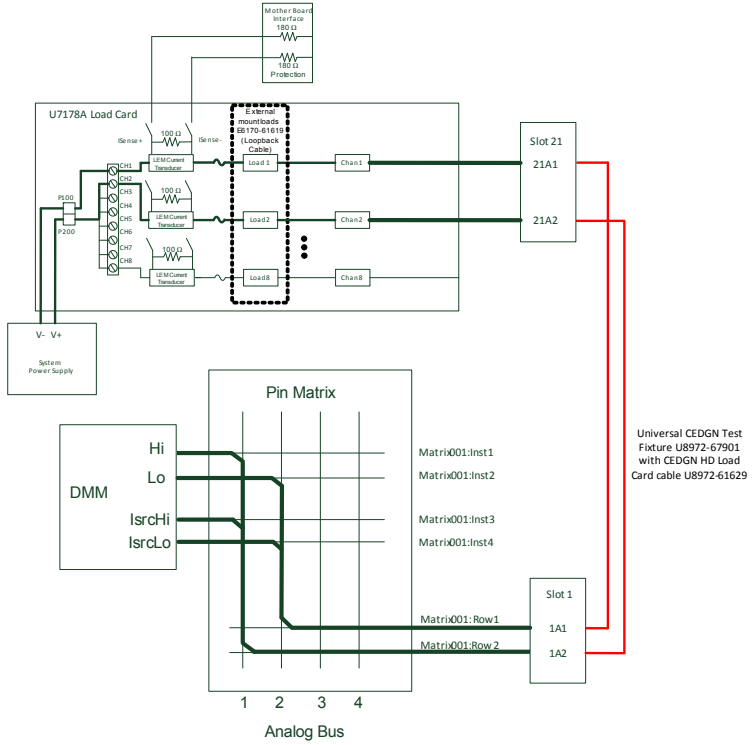
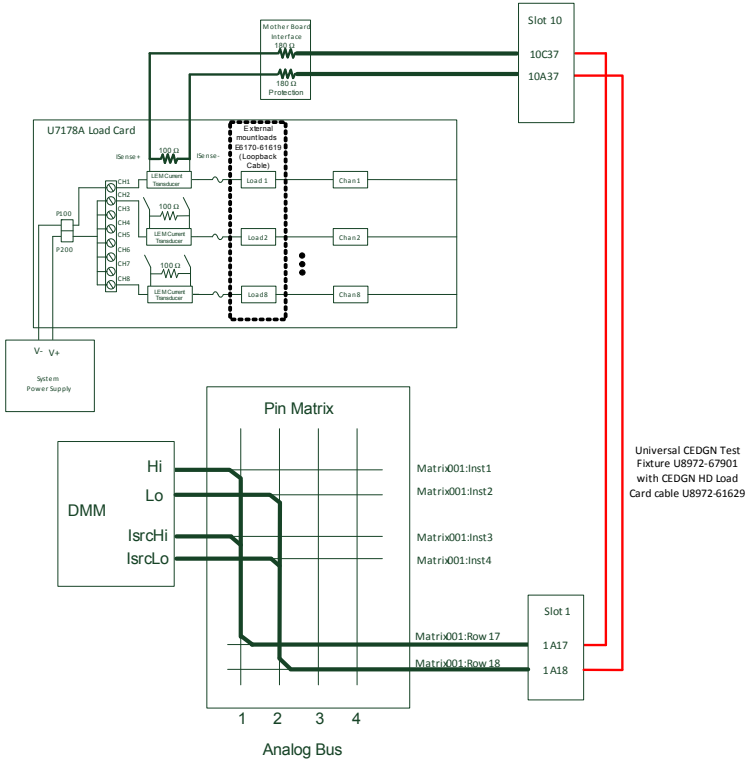


Figure 4-46 U7178A current sense test



Call sequence: *U7179A Load Card test*

- This test sequence verifies the presence of physical connection between U7179A Load Card, power supply and system ICA.
- This test sequence consists of unpowered load card test, powered load card test and current sense test.

- Load relay switches are tested in unpowered load card test. In this test, external mount load with effective load resistance 28.86 Ω (E2240-67012) is mounted on U7179A J1 and J2 connector. Use DMM to measure resistance path between channel 1 and channel 9 via NC and NO, similarly for channel 2 and channel 10, and son on until channel 8 and channel 16. Figure 4-47 illustrates the resistance measurement path for U7179A unpowered load card test.
- Powered load card test requires DUT power supply. If no DUT Power Supply is present, this test will be skipped. DUT power supply is set to output +5 V (current limit at 0.1 A) and DMM will measure the voltage via load card channel, NC and NO. Figure 4-48 illustrates the measurement path for U7179A powered load card test.
- Figure 4-49 illustrates the internal and external switching connections to test U7179A current sense. This test measures the resistance of current sense path via SLU backplane.
- This test sequence requires two U8972-67901 UNIVERSAL CEDGN Test Fixtures and a U8972-61628 CEDGN Load Card Cable. See Figure 3-4 on how to connect the CEDGN kits for this test.

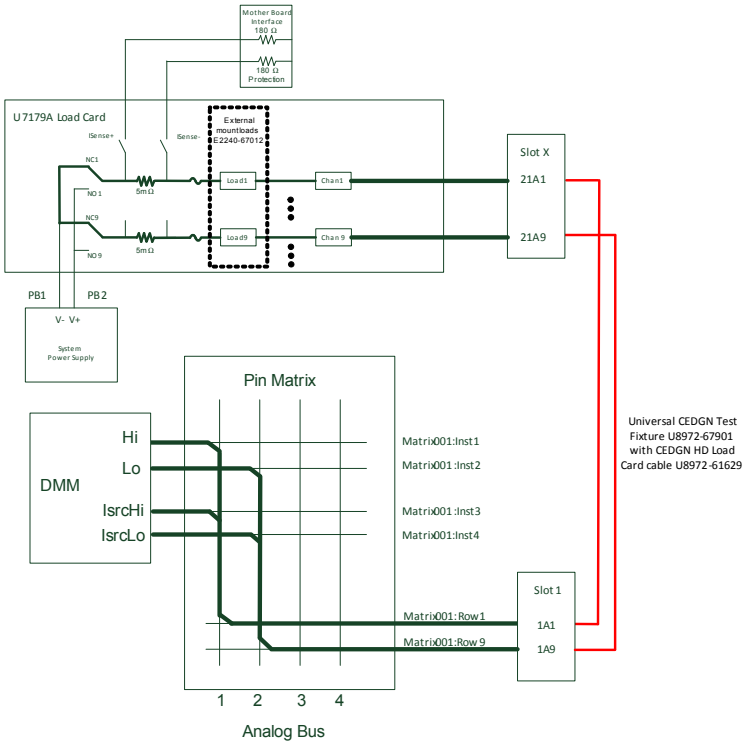


Figure 4-47 U7179A unpowered load card test

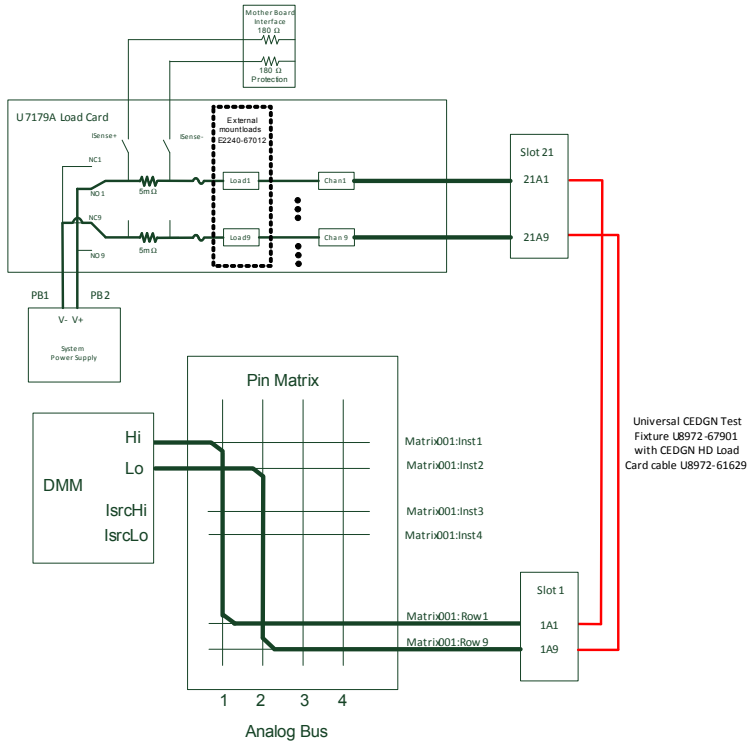


Figure 4-48 U7179A powered load card test

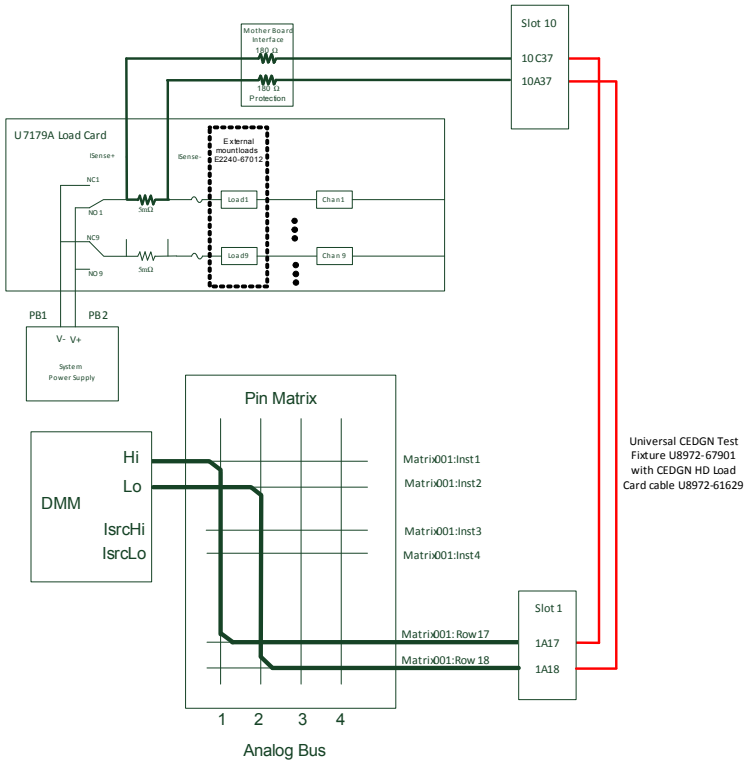


Figure 4-49 U7179A current sense test

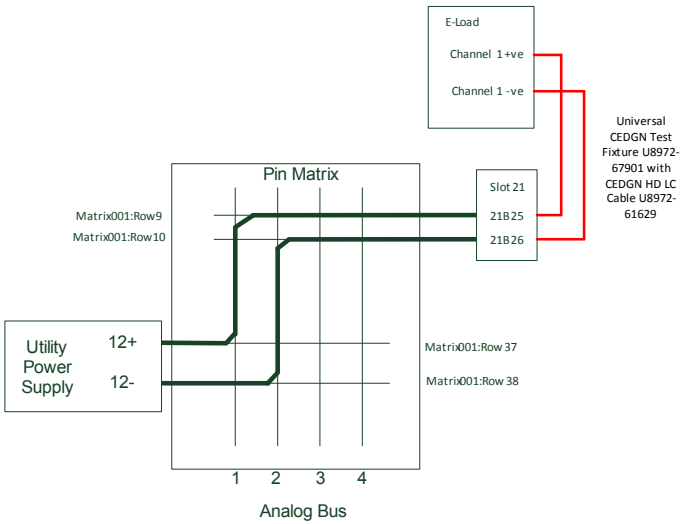
Tests 01800: E-Load Test Group

Call sequence: *E-load test*

- This test sequence verifies the presence of physical connections between electronic load (up to 4 channels) and its basic functions such as mainframe and channel control. In this test, the output of +12V Utility power supply will be connected to the respective e-load channel under test. The e-load channel is expected to read back +12V DC.

- This test requires two U8972-67901 UNIVERSAL CEDGN Test Fixtures, a U8972- 61630 CEDGN E- Load cable, and a U8972-61629 CEDGN HD LC cable. Figure 4-50 illustrates the internal and external connections for this test. See Figure 3-7 on how to connect the CEDGN kits for this test.

Figure 4-50 Measuring utility power supply 12 V using E-Load channel 1 via instrument matrix



Test Fixture Description

U8972-67901 CEDGN Universal Test Fixture

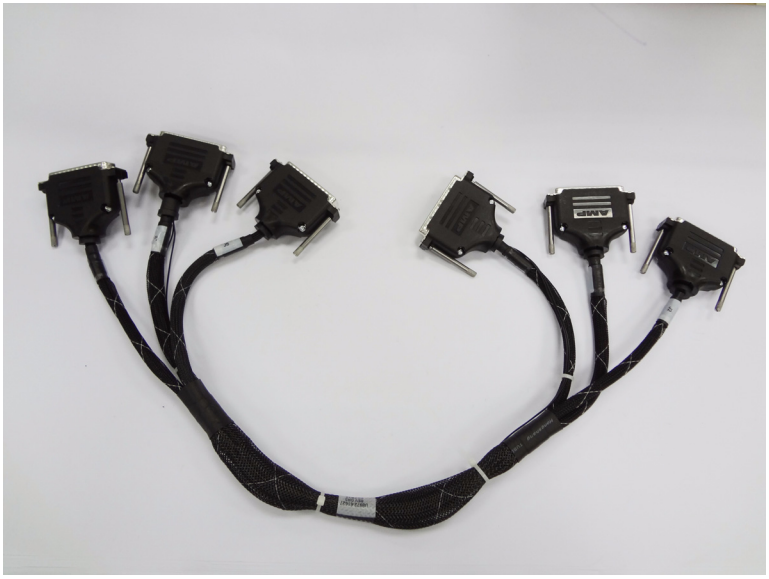
Figure 4-51 CEDGN Universal Test Fixture

U8972-61625 CEDGN PIN MATRIX CABLE

Figure 4-52 CEDGN Loopback Cable (U8972-61625 CEDGN PIN MATRIX CABLE) for E8782A and E8783A Pin Matrix Card Test

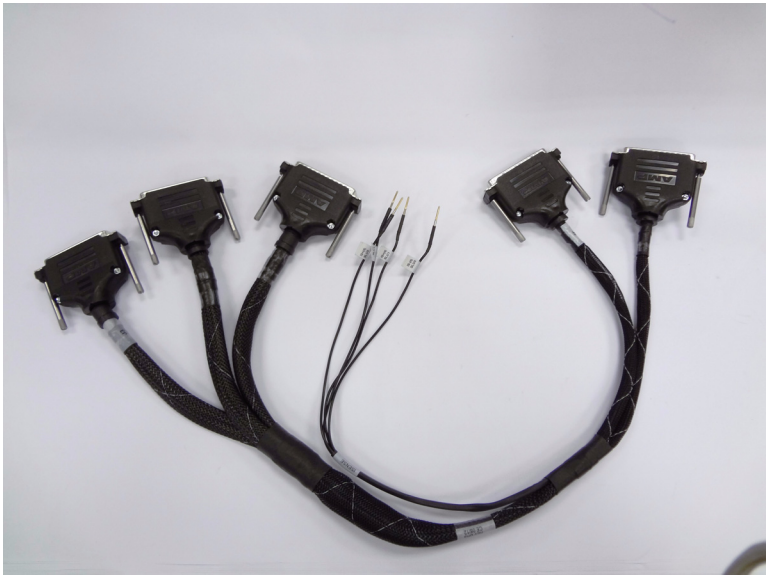
U8972-61627 CEDGN SYSTEM UTILITY CABLE

Figure 4-53 CEDGN Cable (U8972-61627 CEDGN SYSTEM UTILITY CABLE) for System Utility Test



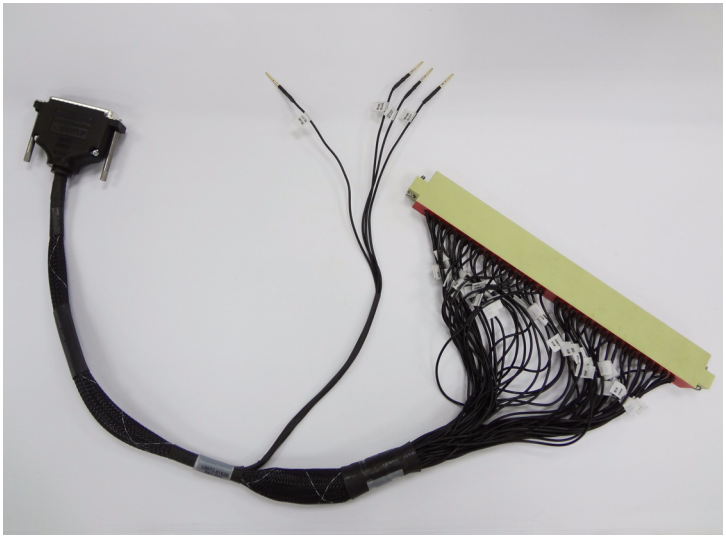
U8972-61628 CEDGN LOAD CARD CABLE

Figure 4-54 CEDGN Cable (U8972-61628 CEDGN LOAD CARD CABLE) for Load Card Test



U8972-61629 CEDGN HD LC CABLE

Figure 4-55 CEDGN Cable (U8972-61629 CEDGN HD LC CABLE) for Heavy Duty Load Card and E-Load Test



U8972-61626 CEDGN HV-DAQ CABLE

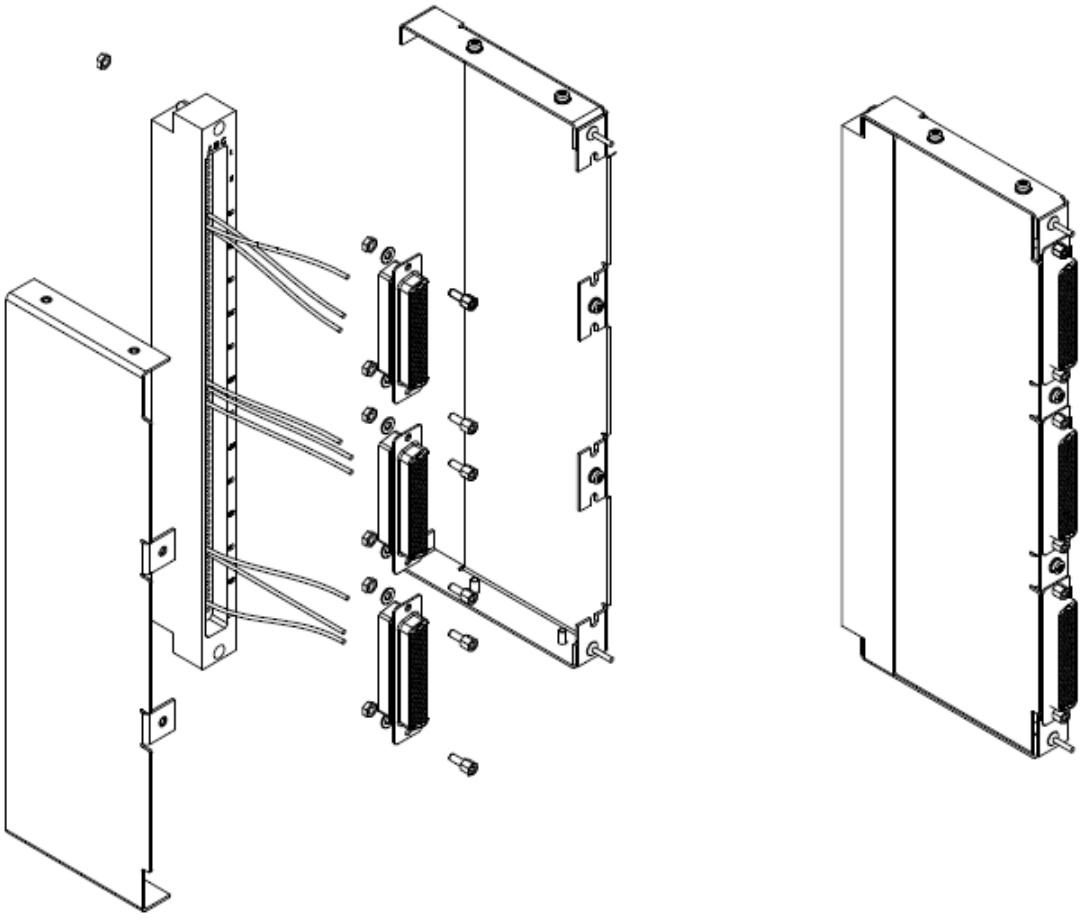
Figure 4-56 CEDGN Cable (U8972-61626 CEDGN HV-DAQ CABLE) for HV-DAQ Test

U8972-61630 CEDGN E-LOAD CABLE

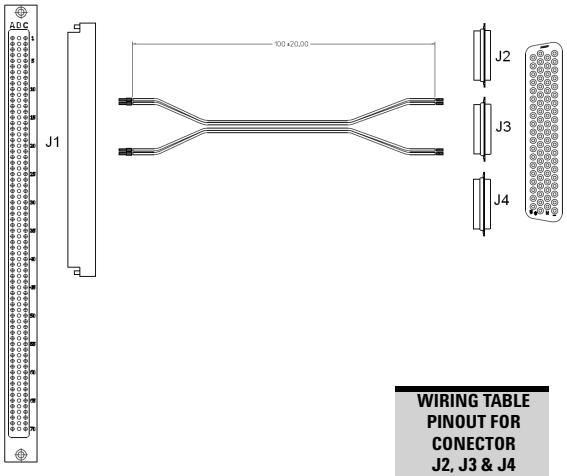
Figure 4-57 CEDGN Cable (U8972-61630 CEDGN E-LOAD CABLE) for E-Load Test

Appendix A
Diagnostic Test Fixture Details

Schematic for U8972-67901 Universal CEDGN Test Fixture



WIRING TABLE PINOUT FOR CONNECTOR J1											
Row	A	Row	B	Row	C	Row	A	Row	B	Row	C
1	J2.1	1	J2.21	1	J2.41	36	J3.16	36	J3.40	36	J3.64
2	J2.2	2	J2.22	2	J2.42	37	J3.17	37	J3.41	37	J3.65
3	J2.3	3	J2.23	3	J2.43	38	J3.18	38	J3.42	38	J3.66
4	J2.4	4	J2.24	4	J2.44	39	J3.19	39	J3.43	39	J3.67
5	J2.5	5	J2.25	5	J2.45	40	J3.20	40	J3.44	40	J3.68
6	J2.6	6	J2.26	6	J2.46	41	J3.21	41	J3.45	41	J3.69
7	J2.7	7	J2.27	7	J2.47	42	J3.22	42	J3.46	42	J3.70
8	J2.8	8	J2.28	8	J2.48	43	J3.23	43	J3.47	43	J3.71
9	J2.9	9	J2.29	9	J2.49	44	J3.24	44	J3.48	44	J3.72
10	J2.10	10	J2.30	10	J2.50	45	J4.1	45	J4.27	45	J4.53
11	J2.11	11	J2.31	11	J2.51	46	J4.2	46	J4.28	46	J4.54
12	J2.12	12	J2.32	12	J2.52	47	J4.3	47	J4.29	47	J4.55
13	J2.13	13	J2.33	13	J2.53	48	J4.4	48	J4.30	48	J4.56
14	J2.14	14	J2.34	14	J2.54	49	J4.5	49	J4.31	49	J4.57
15	J2.15	15	J2.35	15	J2.55	50	J4.6	50	J4.32	50	J4.58
16	J2.16	16	J2.36	16	J2.56	51	J4.7	51	J4.33	51	J4.59
17	J2.17	17	J2.37	17	J2.57	52	J4.8	52	J4.34	52	J4.60
18	J2.18	18	J2.38	18	J2.58	53	J4.9	53	J4.35	53	J4.61
19	J2.19	19	J2.39	19	J2.59	54	J4.10	54	J4.36	54	J4.62
20	J2.20	20	J2.40	20	J2.60	55	J4.11	55	J4.37	55	J4.63
21	J3.1	21	J3.25	21	J3.49	56	J4.12	56	J4.38	56	J4.64
22	J3.2	22	J3.26	22	J3.50	57	J4.13	57	J4.39	57	J4.65
23	J3.3	23	J3.27	23	J3.51	58	J4.14	58	J4.40	58	J4.66
24	J3.4	24	J3.28	24	J3.52	59	J4.15	59	J4.41	59	J4.67
25	J3.5	25	J3.29	25	J3.53	60	J4.16	60	J4.42	60	J4.68
26	J3.6	26	J3.30	26	J3.54	61	J4.17	61	J4.43	61	J4.69
27	J3.7	27	J3.31	27	J3.55	62	J4.18	62	J4.44	62	J4.70
28	J3.8	28	J3.32	28	J3.56	63	J4.19	63	J4.45	63	J4.71
29	J3.9	29	J3.33	29	J3.57	64	J4.20	64	J4.46	64	J4.72
30	J3.10	30	J3.34	30	J3.58	65	J4.21	65	J4.47	65	J4.73
31	J3.11	31	J3.35	31	J3.59	66	J4.22	66	J4.48	66	J4.74
32	J3.12	32	J3.36	32	J3.60	67	J4.23	67	J4.49	67	J4.75
33	J3.13	33	J3.37	33	J3.61	68	J4.24	68	J4.50	68	J4.76
34	J3.14	34	J3.38	34	J3.62	69	J4.25	69	J4.51	69	J4.77
35	J3.15	35	J3.39	35	J3.63	70	J4.26	70	J4.52	70	J4.78

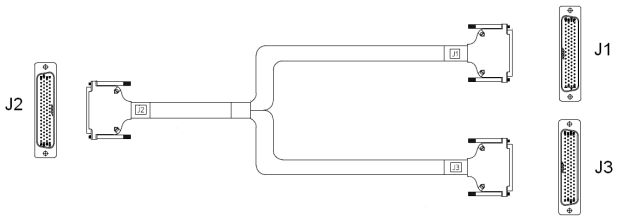


WIRING TABLE PINOUT FOR CONECTOR J2, J3 & J4			
1	21	40	60
2	22	41	61
3	23	42	62
4	24	43	63
5	25	44	64
6	26	45	65
7	27	46	66
8	28	47	67
9	29	48	68
10	30	49	69
11	31	50	70
12	32	51	71
13	33	52	72
14	34	53	73
15	35	54	74
16	36	55	75
17	37	56	76
18	38	57	77
19	39	58	78
20		59	

Schematic for U8972-61625 CEDGN Pin Matrix Cable

PINOUT for J1							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J1-1	row1	J1-21	UUTCom	J1-40	UUTCom	J1-60	aux20
J1-2	row2	J1-22	UUTCom	J1-41	aux1	J1-61	NC
J1-3	row3	J1-23	UUTCom	J1-42	aux2	J1-62	NC
J1-4	row4	J1-24	UUTCom	J1-43	aux3	J1-63	NC
J1-5	row5	J1-25	UUTCom	J1-44	aux4	J1-64	NC
J1-6	row6	J1-26	UUTCom	J1-45	aux5	J1-65	NC
J1-7	row7	J1-27	UUTCom	J1-46	aux6	J1-66	NC
J1-8	row8	J1-28	UUTCom	J1-47	aux7	J1-67	NC
J1-9	row9	J1-29	UUTCom	J1-48	aux8	J1-68	NC
J1-10	row10	J1-30	UUTCom	J1-49	aux9	J1-69	NC
J1-11	row11	J1-31	UUTCom	J1-50	aux10	J1-70	NC
J1-12	row12	J1-32	UUTCom	J1-51	aux11	J1-71	NC
J1-13	row13	J1-33	UUTCom	J1-52	aux12	J1-72	NC
J1-14	row14	J1-34	UUTCom	J1-53	aux13	J1-73	NC
J1-15	row15	J1-35	UUTCom	J1-54	aux14	J1-74	NC
J1-16	row16	J1-36	UUTCom	J1-55	aux15	J1-75	NC
J1-17	row17	J1-37	UUTCom	J1-56	aux16	J1-76	NC
J1-18	row18	J1-38	UUTCom	J1-57	aux17	J1-77	NC
J1-19	row19	J1-39	UUTCom	J1-58	aux18	J1-78	NC
J1-20	row20			J1-59	aux19		

PINOUT for J2							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J2-1	row21	J2-21	row41	J2-40	NC	J2-60	aux32
J2-2	row22	J2-22	row42	J2-41	NC	J2-61	aux33
J2-3	row23	J2-23	row43	J2-42	NC	J2-62	aux34
J2-4	row24	J2-24	row44	J2-43	NC	J2-63	aux35
J2-5	row25	J2-25	UUTCom	J2-44	NC	J2-64	aux36
J2-6	row26	J2-26	UUTCom	J2-45	NC	J2-65	aux37
J2-7	row27	J2-27	UUTCom	J2-46	NC	J2-66	aux38
J2-8	row28	J2-28	UUTCom	J2-47	NC	J2-67	aux39
J2-9	row29	J2-29	UUTCom	J2-48	NC	J2-68	aux40
J2-10	row30	J2-30	UUTCom	J2-49	aux21	J2-69	aux41
J2-11	row31	J2-31	UUTCom	J2-50	aux22	J2-70	aux42
J2-12	row32	J2-32	UUTCom	J2-51	aux23	J2-71	aux43
J2-13	row33	J2-33	UUTCom	J2-52	aux24	J2-72	aux44
J2-14	row34	J2-34	UUTCom	J2-53	aux25	J2-73	NC
J2-15	row35	J2-35	UUTCom	J2-54	aux26	J2-74	NC
J2-16	row36	J2-36	UUTCom	J2-55	aux27	J2-75	NC
J2-17	row37	J2-37	NC	J2-56	aux28	J2-76	NC
J2-18	row38	J2-38	NC	J2-57	aux29	J2-77	NC
J2-19	row39	J2-39	NC	J2-58	aux30	J2-78	NC
J2-20	row40			J2-59	aux31		



PINOUT for J3							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J3-1	row45	J3-21	NC	J3-40	NC	J3-60	aux52
J3-2	row46	J3-22	NC	J3-41	NC	J3-61	aux53
J3-3	row47	J3-23	NC	J3-42	NC	J3-62	aux54
J3-4	row48	J3-24	NC	J3-43	NC	J3-63	aux55
J3-5	row49	J3-25	NC	J3-44	NC	J3-64	aux56
J3-6	row50	J3-26	NC	J3-45	NC	J3-65	aux57
J3-7	row51	J3-27	NC	J3-46	NC	J3-66	aux58
J3-8	row52	J3-28	NC	J3-47	NC	J3-67	aux59
J3-9	row53	J3-29	NC	J3-48	NC	J3-68	aux60
J3-10	row54	J3-30	NC	J3-49	NC	J3-69	aux61
J3-11	row55	J3-31	NC	J3-50	NC	J3-70	aux62
J3-12	row56	J3-32	NC	J3-51	NC	J3-71	aux63
J3-13	row57	J3-33	NC	J3-52	NC	J3-72	aux64
J3-14	row58	J3-34	NC	J3-53	aux45	J3-73	NC
J3-15	row59	J3-35	NC	J3-54	aux46	J3-74	NC
J3-16	row60	J3-36	NC	J3-55	aux47	J3-75	NC
J3-17	row61	J3-37	NC	J3-56	aux48	J3-76	NC
J3-18	row62	J3-38	NC	J3-57	aux49	J3-77	NC
J3-19	row63	J3-39	NC	J3-58	aux50	J3-78	NC
J3-20	row64			J3-59	aux51		

Connect				
From (J1)		To (J1)		Remark
Pin	Name	Pin	Name	
J1-1	row1	J1-2	row2	1 to 1 wire
J1-3	row3	J1-4	row4	1 to 1 wire
J1-5	row5	J1-6	row6	1 to 1 wire
J1-7	row7	J1-8	row8	1 to 1 wire
J1-9	row9	J1-10	row10	1 to 1 wire
J1-11	row11	J1-12	row12	1 to 1 wire
J1-13	row13	J1-14	row14	1 to 1 wire
J1-15	row15	J1-16	row16	1 to 1 wire
J1-17	row17	J1-18	row18	1 to 1 wire
J1-19	row19	J1-20	row20	1 to 1 wire
J1-21	UUTCom	J1-41	aux1	1 to 2 wires
		J1-42	aux2	
J1-22	UUTCom	J1-43	aux3	1 to 2 wires
		J1-44	aux4	
J1-23	UUTCom	J1-45	aux5	1 to 2 wires
		J1-46	aux6	
J1-24	UUTCom	J1-47	aux7	1 to 2 wires
		J1-48	aux8	
J1-25	UUTCom	J1-49	aux9	1 to 2 wires
		J1-50	aux10	
J1-26	UUTCom	J1-51	aux11	1 to 2 wires
		J1-52	aux12	
J1-27	UUTCom	J1-53	aux13	1 to 2 wires
		J1-54	aux14	
J1-28	UUTCom	J1-55	aux15	1 to 2 wires
		J1-56	aux16	
J1-29	UUTCom	J1-57	aux17	1 to 2 wires
		J1-58	aux18	
J1-30	UUTCom	J1-59	aux19	1 to 2 wires
		J1-60	aux20	

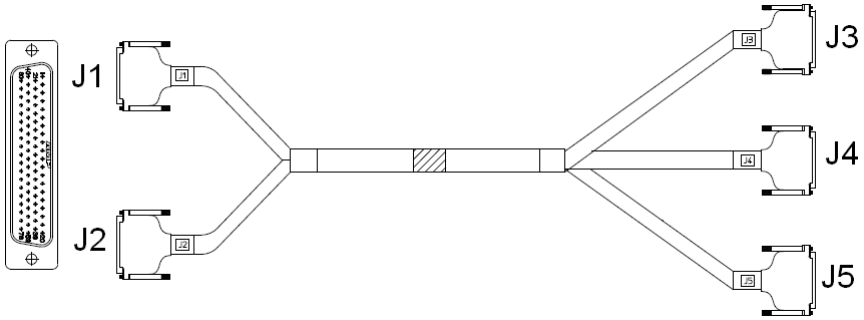
Connect				
From (J3)		To (J3)		Remark
Pin	Name	Pin	Name	
J3-1	row45	J3-2	row46	1 to 1 wire
J3-3	row47	J3-4	row48	1 to 1 wire
J3-5	row49	J3-6	row50	1 to 1 wire
J3-7	row51	J3-8	row52	1 to 1 wire
J3-9	row53	J3-10	row54	1 to 1 wire
J3-11	row55	J3-12	row56	1 to 1 wire
J3-13	row57	J3-14	row58	1 to 1 wire
J3-15	row59	J3-16	row60	1 to 1 wire
J3-17	row61	J3-18	row62	1 to 1 wire
J3-19	row63	J3-20	row64	1 to 1 wire

Connect				
From (J2)		To (J2)		Remark
Pin	Name	Pin	Name	
J2-1	row21	J2-2	row22	1 to 1 wire
J2-3	row23	J2-4	row24	1 to 1 wire
J2-5	row25	J2-6	row26	1 to 1 wire
J2-7	row27	J2-8	row28	1 to 1 wire
J2-9	row29	J2-10	row30	1 to 1 wire
J2-11	row31	J2-12	row32	1 to 1 wire
J2-13	row33	J2-14	row34	1 to 1 wire
J2-15	row35	J2-16	row36	1 to 1 wire
J2-17	row37	J2-18	row38	1 to 1 wire
J2-19	row39	J2-20	row40	1 to 1 wire
J2-21	row41	J2-22	row42	1 to 1 wire
J2-23	row43	J2-24	row44	1 to 1 wire
J2-25	UUTCom	J2-69	aux41	1 to 2 wires
		J2-70	aux42	
J2-26	UUTCom	J2-71	aux43	1 to 2 wires
		J2-72	aux44	

Connect				
From (J1)		To (J2)		Remark
Pin	Name	Pin	Name	
J1-31	UUTCom	J2-49	aux21	1 to 2 wires
		J2-50	aux22	
J1-32	UUTCom	J2-51	aux23	1 to 2 wires
		J2-52	aux24	
J1-33	UUTCom	J2-53	aux25	1 to 2 wires
		J2-54	aux26	
J1-34	UUTCom	J2-55	aux27	1 to 2 wires
		J2-56	aux28	
J1-35	UUTCom	J2-57	aux29	1 to 2 wires
		J2-58	aux30	
J1-36	UUTCom	J2-59	aux31	1 to 2 wires
		J2-60	aux32	
J1-37	UUTCom	J2-61	aux33	1 to 2 wires
		J2-62	aux34	
J1-38	UUTCom	J2-63	aux35	1 to 2 wires
		J2-64	aux36	
J1-39	UUTCom	J2-65	aux37	1 to 2 wires
		J2-66	aux38	
J1-40	UUTCom	J2-67	aux39	1 to 2 wires
		J2-68	aux40	

Connect				
From (J3)		To (J3)		Remark
Pin	Name	Pin	Name	
J2-27	UUTCom	J3-53	aux45	1 to 2 wires
		J3-54	aux46	
J2-28	UUTCom	J3-55	aux47	1 to 2 wires
		J3-56	aux48	
J2-29	UUTCom	J3-57	aux49	1 to 2 wires
		J3-58	aux50	
J2-30	UUTCom	J3-59	aux51	1 to 2 wires
		J3-60	aux52	
J2-31	UUTCom	J3-61	aux53	1 to 2 wires
		J3-62	aux54	
J2-32	UUTCom	J3-63	aux55	1 to 2 wires
		J3-64	aux56	
J2-33	UUTCom	J3-65	aux57	1 to 2 wires
		J3-66	aux58	
J2-34	UUTCom	J3-67	aux59	1 to 2 wires
		J3-68	aux60	
J2-35	UUTCom	J3-69	aux61	1 to 2 wires
		J3-70	aux62	
J2-36	UUTCom	J3-71	aux63	1 to 2 wires
		J3-72	aux64	

Schematic for U8972-61626 CEDGN HV-DAQ CABL



PINOUT for J1											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J1-1	row1	DAQ1.Port 1 & DAQ2.Port 1	J1-21		NC	J1-40		NC	J1-60		NC
J1-2	row2	DAQ1.Port 2 & DAQ2.Port 2	J1-22		NC	J1-41		NC	J1-61		NC
J1-3	row3	DAQ1.Port 3 & DAQ2.Port 3	J1-23		NC	J1-42	aux2	DAQ1.Aux11 & DAQ2.Aux11	J1-62		NC
J1-4	row4	DAQ1.Port 4 & DAQ2.Port 4	J1-24		NC	J1-43	aux3	DAQ1.Aux21 & DAQ2.Aux21	J1-63		NC
J1-5	row5	DAQ1.Port 5 & DAQ2.Port 5	J1-25		NC	J1-44	aux4	DAQ1.Aux31 & DAQ2.Aux31	J1-64		NC
J1-6	row6	DAQ1.Port 6 & DAQ2.Port 6	J1-26		NC	J1-45	aux5	DAQ1.Aux41 & DAQ2.Aux41	J1-65		NC
J1-7	row7	DAQ1.Port 7 & DAQ2.Port 7	J1-27		NC	J1-46	aux6	DAQ1.Aux51 & DAQ2.Aux51	J1-66		NC
J1-8	row8	DAQ1.Port 8 & DAQ2.Port 8	J1-28		NC	J1-47	aux7	DAQ1.Aux61 & DAQ2.Aux61	J1-67		NC
J1-9	row9	DAQ1.Port 9 & DAQ2.Port 9	J1-29		NC	J1-48	aux8	DAQ1.Aux71 & DAQ2.Aux71	J1-68		NC
J1-10	row10	DAQ1.Port 10 & DAQ2.Port 10	J1-30		NC	J1-49	aux9	DAQ1.Aux81 & DAQ2.Aux81	J1-69		NC
J1-11	row11	DAQ1.Port 11 & DAQ2.Port 11	J1-31		NC	J1-50	aux10	DAQ1.Aux12 & DAQ2.Aux12	J1-70		NC
J1-12	row12	DAQ1.Port 12 & DAQ2.Port 12	J1-32		NC	J1-51	aux11	DAQ1.Aux22 & DAQ2.Aux22	J1-71		NC
J1-13	row13	DAQ1.Port 13 & DAQ2.Port 13	J1-33		NC	J1-52	aux12	DAQ1.Aux32 & DAQ2.Aux32	J1-72		NC
J1-14	row14	DAQ1.Port 14 & DAQ2.Port 14	J1-34		NC	J1-53	aux13	DAQ1.Aux42 & DAQ2.Aux42	J1-73		NC
J1-15	row15	DAQ1.Port 15 & DAQ2.Port 15	J1-35		NC	J1-54	aux14	DAQ1.Aux52 & DAQ2.Aux52	J1-74		NC
J1-16	row16	DAQ1.Port 16 & DAQ2.Port 16	J1-36		NC	J1-55	aux15	DAQ1.Aux62 & DAQ2.Aux62	J1-75		NC
J1-17	row17	DAQ1.Port 17 & DAQ2.Port 17	J1-37		NC	J1-56	aux16	DAQ1.Aux72 & DAQ2.Aux72	J1-76		NC
J1-18	row18	DAQ1.Port 18 & DAQ2.Port 18	J1-38		NC	J1-57	aux17	DAQ1.Aux82 & DAQ2.Aux82	J1-77		NC
J1-19	row19	DAQ1.Port 19 & DAQ2.Port 19	J1-39		NC	J1-58		NC	J1-78		NC
J1-20	row20	DAQ1.Port 20 & DAQ2.Port 20			NC	J1-59		NC			

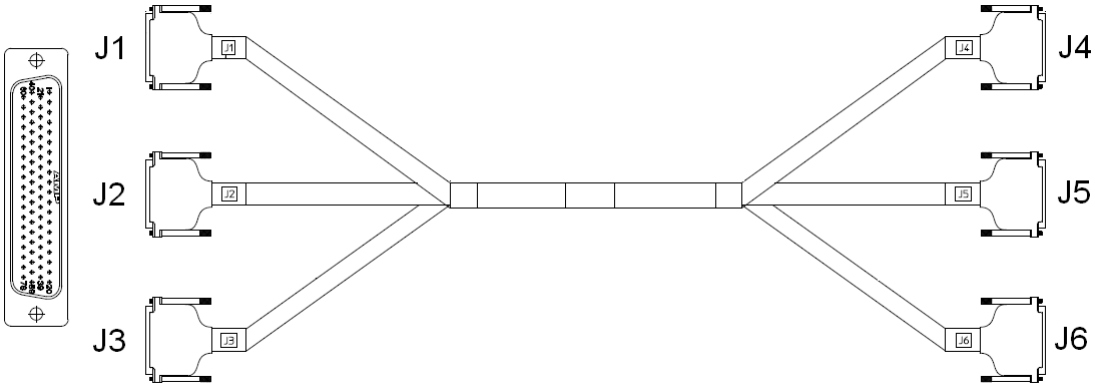
PINOUT for J2											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J2-1	row21	DAQ1.Port 21 & DAQ2.Port 21	J2-21		NC	J2-40		NC	J2-60		NC
J2-2	row22	DAQ1.Port 22 & DAQ2.Port 22	J2-22		NC	J2-41		NC	J2-61		NC
J2-3	row23	DAQ1.Port 23 & DAQ2.Port 23	J2-23		NC	J2-42		NC	J2-62		NC
J2-4	row24	DAQ1.Port 24 & DAQ2.Port 24	J2-24		NC	J2-43		NC	J2-63		NC
J2-5	row25	DAQ1.Port 25 & DAQ2.Port 25	J2-25		NC	J2-44		NC	J2-64		NC
J2-6	row26	DAQ1.Port 26 & DAQ2.Port 26	J2-26		NC	J2-45		NC	J2-65		NC
J2-7	row27	DAQ1.Port 27 & DAQ2.Port 27	J2-27		NC	J2-46		NC	J2-66		NC
J2-8	row28	DAQ1.Port 28 & DAQ2.Port 28	J2-28		NC	J2-47		NC	J2-67		NC
J2-9	row29	DAQ1.Port 29 & DAQ2.Port 29	J2-29		NC	J2-48		NC	J2-68		NC
J2-10	row30	DAQ1.Port 30 & DAQ2.Port 30	J2-30		NC	J2-49		NC	J2-69		NC
J2-11	row31	DAQ1.Port 31 & DAQ2.Port 31	J2-31		NC	J2-50		NC	J2-70		NC
J2-12	row32	DAQ1.Port 32 & DAQ2.Port 32	J2-32		NC	J2-51		NC	J2-71		NC
J2-13	row33	DAQ1.G1	J2-33		NC	J2-52		NC	J2-72		NC
J2-14	row34	DAQ1.G2	J2-34		NC	J2-53		NC	J2-73		NC
J2-15	row35	DAQ1.G3	J2-35		NC	J2-54		NC	J2-74		NC
J2-16	row36	DAQ1.G4	J2-36		NC	J2-55		NC	J2-75		NC
J2-17	row37	DAQ2.G1	J2-37		NC	J2-56		NC	J2-76		NC
J2-18	row38	DAQ2.G2	J2-38		NC	J2-57		NC	J2-77		NC
J2-19	row39	DAQ2.G3	J2-39		NC	J2-58		NC	J2-78		NC
J2-20	row40	DAQ2.G4				J2-59		NC			

PINOUT for J3							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J3-1	DAQ1.Port 1	J3-21	DAQ1.G1	J3-40	NC	J3-60	DAQ1.Aux42
J3-2	DAQ1.Port 9	J3-22	DAQ1.G1	J3-41	DAQ1.Port 2	J3-61	NC
J3-3	DAQ1.Port 17	J3-23	DAQ1.G1	J3-42	DAQ1.Port 10	J3-62	NC
J3-4	DAQ1.Port 25	J3-24	DAQ1.G1	J3-43	DAQ1.Port 18	J3-63	NC
J3-5	DAQ1.Port 3	J3-25	DAQ1.G2	J3-44	DAQ1.Port 26	J3-64	NC
J3-6	DAQ1.Port 11	J3-26	DAQ1.G2	J3-45	DAQ1.Port 4	J3-65	NC
J3-7	DAQ1.Port 19	J3-27	DAQ1.G2	J3-46	DAQ1.Port 12	J3-66	NC
J3-8	DAQ1.Port 27	J3-28	DAQ1.G2	J3-47	DAQ1.Port 20	J3-67	NC
J3-9	DAQ1.Port 5	J3-29	DAQ1.G3	J3-48	DAQ1.Port 28	J3-68	NC
J3-10	DAQ1.Port 13	J3-30	DAQ1.G3	J3-49	DAQ1.Port 6	J3-69	NC
J3-11	DAQ1.Port 21	J3-31	DAQ1.G3	J3-50	DAQ1.Port 14	J3-70	NC
J3-12	DAQ1.Port 29	J3-32	DAQ1.G3	J3-51	DAQ1.Port 22	J3-71	NC
J3-13	DAQ1.Port 7	J3-33	DAQ1.G4	J3-52	DAQ1.Port 30	J3-72	NC
J3-14	DAQ1.Port 15	J3-34	DAQ1.G4	J3-53	DAQ1.Port 8	J3-73	NC
J3-15	DAQ1.Port 23	J3-35	DAQ1.G4	J3-54	DAQ1.Port 16	J3-74	NC
J3-16	DAQ1.Port 31	J3-36	DAQ1.G4	J3-55	DAQ1.Port 24	J3-75	NC
J3-17	DAQ1.Aux11	J3-37	NC	J3-56	DAQ1.Port 32	J3-76	NC
J3-18	DAQ1.Aux21	J3-38	NC	J3-57	DAQ1.Aux12	J3-77	NC
J3-19	DAQ1.Aux31	J3-39	NC	J3-58	DAQ1.Aux22	J3-78	NC
J3-20	DAQ1.Aux41			J3-59	DAQ1.Aux32		

PINOUT for J4							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J4-1	DAQ1.Aux51	J4-21	NC	J4-40	NC	J4-60	NC
J4-2	DAQ1.Aux61	J4-22	NC	J4-41	NC	J4-61	NC
J4-3	DAQ1.Aux71	J4-23	NC	J4-42	NC	J4-62	NC
J4-4	DAQ1.Aux81	J4-24	NC	J4-43	NC	J4-63	NC
J4-5	NC	J4-25	NC	J4-44	NC	J4-64	NC
J4-6	NC	J4-26	NC	J4-45	NC	J4-65	NC
J4-7	NC	J4-27	NC	J4-46	NC	J4-66	NC
J4-8	NC	J4-28	NC	J4-47	NC	J4-67	NC
J4-9	NC	J4-29	NC	J4-48	NC	J4-68	NC
J4-10	NC	J4-30	NC	J4-49	DAQ1.Aux52	J4-69	NC
J4-11	NC	J4-31	NC	J4-50	DAQ1.Aux62	J4-70	NC
J4-12	NC	J4-32	NC	J4-51	DAQ1.Aux72	J4-71	NC
J4-13	NC	J4-33	NC	J4-52	DAQ1.Aux82	J4-72	NC
J4-14	NC	J4-34	NC	J4-53	NC	J4-73	NC
J4-15	NC	J4-35	NC	J4-54	NC	J4-74	NC
J4-16	NC	J4-36	NC	J4-55	NC	J4-75	NC
J4-17	NC	J4-37	NC	J4-56	NC	J4-76	NC
J4-18	NC	J4-38	NC	J4-57	NC	J4-77	NC
J4-19	NC	J4-39	NC	J4-58	NC	J4-78	NC
J4-20	NC			J4-59	NC		

PINOUT for J5							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J5-1	NC	J5-21	DAQ2.Aux31	J5-40	DAQ2.G3	J5-60	DAQ2.Port 12
J5-2	NC	J5-22	DAQ2.Aux41	J5-41	DAQ2.G4	J5-61	DAQ2.Port 20
J5-3	DAQ2.Port 1	J5-23	DAQ2.Aux51	J5-42	DAQ2.G4	J5-62	DAQ2.Port 28
J5-4	DAQ2.Port 9	J5-24	DAQ2.Aux61	J5-43	DAQ2.G4	J5-63	DAQ2.Port 6
J5-5	DAQ2.Port 17	J5-25	DAQ2.Aux71	J5-44	DAQ2.G4	J5-64	DAQ2.Port 14
J5-6	DAQ2.Port 25	J5-26	DAQ2.Aux81	J5-45	NC	J5-65	DAQ2.Port 22
J5-7	DAQ2.Port 3	J5-27	NC	J5-46	NC	J5-66	DAQ2.Port 30
J5-8	DAQ2.Port 11	J5-28	NC	J5-47	NC	J5-67	DAQ2.Port 8
J5-9	DAQ2.Port 19	J5-29	DAQ2.G1	J5-48	NC	J5-68	DAQ2.Port 16
J5-10	DAQ2.Port 27	J5-30	DAQ2.G1	J5-49	NC	J5-69	DAQ2.Port 24
J5-11	DAQ2.Port 5	J5-31	DAQ2.G1	J5-50	NC	J5-70	DAQ2.Port 32
J5-12	DAQ2.Port 13	J5-32	DAQ2.G1	J5-51	NC	J5-71	DAQ2.Aux12
J5-13	DAQ2.Port 21	J5-33	DAQ2.G2	J5-52	NC	J5-72	DAQ2.Aux22
J5-14	DAQ2.Port 29	J5-34	DAQ2.G2	J5-53	NC	J5-73	DAQ2.Aux32
J5-15	DAQ2.Port 7	J5-35	DAQ2.G2	J5-54	NC	J5-74	DAQ2.Aux42
J5-16	DAQ2.Port 15	J5-36	DAQ2.G2	J5-55	DAQ2.Port 2	J5-75	DAQ2.Aux52
J5-17	DAQ2.Port 23	J5-37	DAQ2.G3	J5-56	DAQ2.Port 10	J5-76	DAQ2.Aux62
J5-18	DAQ2.Port 31	J5-38	DAQ2.G3	J5-57	DAQ2.Port 18	J5-77	DAQ2.Aux72
J5-19	DAQ2.Aux11	J5-39	DAQ2.G3	J5-58	DAQ2.Port 26	J5-78	DAQ2.Aux82
J5-20	DAQ2.Aux21			J5-59	DAQ2.Port 4		

Schematic for U8972-61627 CEDGN System Utility Cable



PINOUT for J1											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J1-1	row1	J4-9	J1-21	UUTCom	J4-29	J1-40		NC	J1-60		NC
J1-2	row2	J4-49	J1-22	UUTCom	J4-30	J1-41		NC	J1-61		NC
J1-3	row3	J4-10	J1-23		NC	J1-42		NC	J1-62		NC
J1-4	row4	J4-50	J1-24		NC	J1-43		NC	J1-63		NC
J1-5	row5	J4-11	J1-25	UUTCom	J4-31	J1-44		NC	J1-64		NC
J1-6	row6	J4-51	J1-26	UUTCom	J4-32	J1-45		NC	J1-65		NC
J1-7	row7	J4-12	J1-27		NC	J1-46		NC	J1-66		NC
J1-8	row8	J4-52	J1-28		NC	J1-47		NC	J1-67		NC
J1-9	row9	J4-13	J1-29		NC	J1-48		NC	J1-68		NC
J1-10	row10	J4-33	J1-30		NC	J1-49		NC	J1-69		NC
J1-11	row11	J4-14	J1-31		NC	J1-50		NC	J1-70		NC
J1-12	row12	J4-34	J1-32		NC	J1-51		NC	J1-71		NC
J1-13	row13	J4-15	J1-33		NC	J1-52		NC	J1-72		NC
J1-14	row14	J4-35	J1-34		NC	J1-53		NC	J1-73		NC
J1-15	row15	J4-16	J1-35		NC	J1-54		NC	J1-74		NC
J1-16	row16	J4-36	J1-36		NC	J1-55		NC	J1-75		NC
J1-17	row17	J4-17	J1-37		NC	J1-56		NC	J1-76		NC
J1-18	row18	J4-37	J1-38		NC	J1-57		NC	J1-77		NC
J1-19	row19	NC	J1-39		NC	J1-58		NC	J1-78		NC
J1-20	row20	NC				J1-59		NC			

PINOUT for J2											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J2-1	row1	J4-20	J2-21		NC	J2-40		NC	J2-60		NC
J2-2	row2	J5-5	J2-22		NC	J2-41		NC	J2-61		NC
J2-3	row3	J4-60	J2-23		NC	J2-42		NC	J2-62		NC
J2-4	row4	J5-53	J2-24		NC	J2-43		NC	J2-63		NC
J2-5	row5	J5-14	J2-25		NC	J2-44		NC	J2-64		NC
J2-6	row6	J5-15	J2-26		NC	J2-45		NC	J2-65		NC
J2-7	row7	J5-16	J2-27		NC	J2-46		NC	J2-66		NC
J2-8	row8	J5-17	J2-28		NC	J2-47		NC	J2-67		NC
J2-9	row9	J5-62	J2-29		NC	J2-48		NC	J2-68		NC
J2-10	row10	J5-63	J2-30		NC	J2-49		NC	J2-69		NC
J2-11	row11	J5-64	J2-31		NC	J2-50		NC	J2-70		NC
J2-12	row12	J5-65	J2-32		NC	J2-51		NC	J2-71		NC
J2-13	row13	J5-18	J2-33		NC	J2-52		NC	J2-72		NC
J2-14	row14	J5-66	J2-34		NC	J2-53		NC	J2-73		NC
J2-15	row15	J5-19	J2-35		NC	J2-54		NC	J2-74		NC
J2-16	row16	J5-67	J2-36		NC	J2-55		NC	J2-75		NC
J2-17	row17	J5-24	J2-37		NC	J2-56		NC	J2-76		NC
J2-18	row18	J6-1	J2-38		NC	J2-57		NC	J2-77		NC
J2-19	row19	J6-2	J2-39		NC	J2-58		NC	J2-78		NC
J2-20	row20	J6-3				J2-59		NC			

PINOUT for J3											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J3-1	row21	J5-72	J3-21		NC	J3-40		NC	J3-60		NC
J3-2	row22	J6-53	J3-22		NC	J3-41		NC	J3-61		NC
J3-3	row23	J6-54	J3-23		NC	J3-42		NC	J3-62		NC
J3-4	row24	J6-55	J3-24		NC	J3-43		NC	J3-63		NC
J3-5	row25	J6-4	J3-25		NC	J3-44		NC	J3-64		NC
J3-6	row26	J6-56	J3-26		NC	J3-45		NC	J3-65		NC
J3-7	row27	J6-5	J3-27		NC	J3-46		NC	J3-66		NC
J3-8	row28	J6-57	J3-28		NC	J3-47		NC	J3-67		NC
J3-9	row29	J6-16	J3-29	UUTCom	J6-68	J3-48		NC	J3-68		NC
J3-10	row30	J6-17	J3-30	UUTCom	J6-69	J3-49		NC	J3-69		NC
J3-11	row31	J6-18	J3-31	UUTCom	J6-70	J3-50		NC	J3-70		NC
J3-12	row32	J6-19	J3-32	UUTCom	J6-71	J3-51		NC	J3-71		NC
J3-13	row33	J6-20	J3-33	UUTCom	J6-72	J3-52		NC	J3-72		NC
J3-14	row34	J6-21	J3-34	UUTCom	J6-73	J3-53		NC	J3-73		NC
J3-15	row35	J6-22	J3-35	UUTCom	J6-74	J3-54		NC	J3-74		NC
J3-16	row36	J6-23	J3-36	UUTCom	J6-75	J3-55		NC	J3-75		NC
J3-17	row37	J6-25	J3-37		NC	J3-56		NC	J3-76		NC
J3-18	row38	J6-26	J3-38		NC	J3-57		NC	J3-77		NC
J3-19	row39	J6-77	J3-39		NC	J3-58		NC	J3-78		NC
J3-20	row40	J6-78				J3-59		NC			

PINOUT for J4							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J4-1	NC	J4-21	com1 Rx	J4-40	NC	J4-60	System Gnd
J4-2	com1 CD	J4-22	com1 DTR	J4-41	com1 Tx	J4-61	NC
J4-3	com1 RTS	J4-23	com1 CTS	J4-42	com1 DSR	J4-62	NC
J4-4	NC	J4-24	com2 Rx	J4-43	NC	J4-63	NC
J4-5	com2 CD	J4-25	com2 DTR	J4-44	com2 Tx	J4-64	NC
J4-6	com2 RTS	J4-26	com2 CTS	J4-45	com2 DSR	J4-65	NC
J4-7	CAN1.1(+)	J4-27	CAN1.1(-)	J4-46	NC	J4-66	NC
J4-8	CAN1.2(+)	J4-28	CAN1.2(-)	J4-47	CAN1.1(shield)	J4-67	NC
J4-9	DAC1 DMM_H	J4-29	DAC1 ZGNDCAL	J4-48	CAN1.2(shield)	J4-68	NC
J4-10	DAC1 DMM_L	J4-30	DAC1 ZGNDF	J4-49	DAC1 DMM_C	J4-69	NC
J4-11	DAC2 DMM_H	J4-31	DAC2 ZGNDCAL	J4-50	DAC1 TRIGGER	J4-70	NC
J4-12	DAC2 DMM_L	J4-32	DAC2 ZGNDF	J4-51	DAC2 DMM_C	J4-71	NC
J4-13	Spare Instrument(+)	J4-33	Spare Instrument(-)	J4-52	DAC2 TRIGGER	J4-72	NC
J4-14	Spare Instrument(+)	J4-34	Spare Instrument(-)	J4-53	Spare Instrument(shield)	J4-73	NC
J4-15	Spare Instrument(+)	J4-35	Spare Instrument(-)	J4-54	Spare Instrument(shield)	J4-74	NC
J4-16	Spare Instrument(+)	J4-36	Spare Instrument(-)	J4-55	Spare Instrument(shield)	J4-75	NC
J4-17	Spare Instrument(+)	J4-37	Spare Instrument(-)	J4-56	Spare Instrument(shield)	J4-76	NC
J4-18	TX+	J4-38	NC	J4-57	Spare Instrument(shield)	J4-77	NC
J4-19	RX+	J4-39	NC	J4-58	TX-	J4-78	NC
J4-20	System Gnd			J4-59	RX-		

PINOUT for J5							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J5-1	Fixture ID (0)	J5-21	Open Drain Out (2)	J5-40	NC	J5-60	Spare_DigOut (5)
J5-2	Fixture ID (2)	J5-22	Open Drain Out (4)	J5-41	PCI1750 DI	J5-61	Spare_DigOut (7)
J5-3	Fixture ID (4)	J5-23	Open Drain Out (6)	J5-42	PCI1750 DI	J5-62	Isense+ (1)
J5-4	Fixture ID (6)	J5-24	Isense- (1)	J5-43	PCI1750 DI	J5-63	Isense+ (2)
J5-5	System Gnd	J5-25	NC	J5-44	PCI1750 DI	J5-64	Isense+ (3)
J5-6	Digital In (0)	J5-26	NC	J5-45	PCI1750 DI	J5-65	Isense+ (4)
J5-7	Digital In (2)	J5-27	NC	J5-46	PCI1750 DI	J5-66	PB Sense (2)
J5-8	Digital In (4)	J5-28	NC	J5-47	PCI1750 DI	J5-67	PB Sense (4)
J5-9	Digital In (6)	J5-29	NC	J5-48	PCI1750 DI	J5-68	Open Drain Out (1)
J5-10	Spare_DigOut (0)	J5-30	NC	J5-49	Fixture ID (1)	J5-69	Open Drain Out (3)
J5-11	Spare_DigOut (2)	J5-31	NC	J5-50	Fixture ID (3)	J5-70	Open Drain Out (5)
J5-12	Spare_DigOut (4)	J5-32	NC	J5-51	Fixture ID (5)	J5-71	Open Drain Out (7)
J5-13	Spare_DigOut (6)	J5-33	NC	J5-52	Fixture ID (7)	J5-72	Isense+ (1)
J5-14	Isense- (1)	J5-34	NC	J5-53	System Gnd	J5-73	NC
J5-15	Isense- (2)	J5-35	NC	J5-54	Digital In (1)	J5-74	NC
J5-16	Isense- (3)	J5-36	NC	J5-55	Digital In (3)	J5-75	NC
J5-17	Isense- (4)	J5-37	NC	J5-56	Digital In (5)	J5-76	NC
J5-18	PB Sense (1)	J5-38	NC	J5-57	Digital In (7)	J5-77	NC
J5-19	PB Sense (3)	J5-39	NC	J5-58	Spare_DigOut (1)	J5-78	NC
J5-20	Open Drain Out (0)			J5-59	Spare_DigOut (3)		

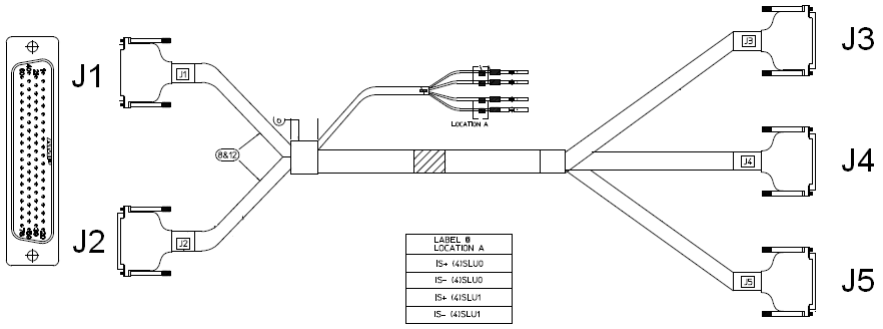
PINOUT for J6							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J6-1	Isense- (2)	J6-21	PS_CH3S+	J6-40	PCI1750 DO	J6-60	NC
J6-2	Isense- (3)	J6-22	PS_CH4+	J6-41	PCI1750 DO	J6-61	NC
J6-3	Isense- (4)	J6-23	PS_CH4S+	J6-42	PCI1750 DO	J6-62	NC
J6-4	PB Sense (1)	J6-24	interlock	J6-43	PCI1750 DO	J6-63	NC
J6-5	PB Sense (3)	J6-25	+12Vdc Supply	J6-44	PCI1750 DO	J6-64	NC
J6-6	NC	J6-26	-12Vdc Supply	J6-45	PCI1750 DO	J6-65	NC
J6-7	NC	J6-27	PCI1750 DI	J6-46	PCI1750 DO	J6-66	NC
J6-8	NC	J6-28	PCI1750 DI	J6-47	PCI1750 DO	J6-67	NC
J6-9	NC	J6-29	PCI1750 DI	J6-48	PCI1750 DO	J6-68	PS_CH1-
J6-10	NC	J6-30	PCI1750 DI	J6-49	PCI1750 DO	J6-69	PS_CH1S-
J6-11	NC	J6-31	PCI1750 DI	J6-50	PCI1750 DO	J6-70	PS_CH2-
J6-12	NC	J6-32	PCI1750 DI	J6-51	PCI1750COM	J6-71	PS_CH2S-
J6-13	NC	J6-33	PCI1750 DI	J6-52	PCI1750IGND	J6-72	PS_CH3-
J6-14	NC	J6-34	PCI1750 DI	J6-53	Isense+ (2)	J6-73	PS_CH3S-
J6-15	NC	J6-35	PCI1750 DO	J6-54	Isense+ (3)	J6-74	PS_CH4-
J6-16	PS_CH1+	J6-36	PCI1750 DO	J6-55	Isense+ (4)	J6-75	PS_CH4S-
J6-17	PS_CH1S+	J6-37	PCI1750 DO	J6-56	PB Sense (2)	J6-76	DCOM
J6-18	PS_CH2+	J6-38	PCI1750 DO	J6-57	PB Sense (4)	J6-77	+24Vdc Supply
J6-19	PS_CH2S+	J6-39	PCI1750 DO	J6-58	NC	J6-78	-24Vdc Supply
J6-20	PS_CH3+			J6-59	NC		

Loopback Wire connection			
From		To	
Pin	Name	Pin	Name
J4-21	com1 Rx	J4-41	com1 Tx
J4-3	com1 RTS	J4-23	com1 CTS
J4-2	com1 CD	J4-42	com1 DSR
J4-22	com1 DTR		
J4-24	com2 Rx	J4-44	com2 Tx
J4-6	com2 RTS	J4-26	com2 CTS
J4-5	com2 CD	J4-45	com2 DSR
J4-25	com2 DTR		
J4-7	CAN1.1(+)	J4-8	CAN1.2(+)
J4-27	CAN1.1(-)	J4-28	CAN1.2(-)
J4-47	CAN1.1(shield)	J4-48	CAN1.2(shield)
J4-18	TX+	J4-19	RX+
J4-58	TX-	J4-59	RX-
J5-41	PCI1750 DI0	J6-35	PCI1750 DO0
J5-42	PCI1750 DI1	J6-36	PCI1750 DO1
J5-43	PCI1750 DI2	J6-37	PCI1750 DO2

Loopback Wire connection			
From		To	
Pin	Name	Pin	Name
J5-44	PCI1750 DI3	J6-38	PCI1750 DO3
J5-45	PCI1750 DI4	J6-39	PCI1750 DO4
J5-46	PCI1750 DI5	J6-40	PCI1750 DO5
J5-47	PCI1750 DI6	J6-41	PCI1750 DO6
J5-48	PCI1750 DI7	J6-42	PCI1750 DO7
J6-27	PCI1750 DI8	J6-43	PCI1750 DO8
J6-28	PCI1750 DI9	J6-44	PCI1750 DO9
J6-29	PCI1750 DI10	J6-45	PCI1750 DO10
J6-30	PCI1750 DI11	J6-46	PCI1750 DO11
J6-31	PCI1750 DI12	J6-47	PCI1750 DO12
J6-32	PCI1750 DI13	J6-48	PCI1750 DO13
J6-33	PCI1750 DI14	J6-49	PCI1750 DO14
J6-34	PCI1750 DI15	J6-50	PCI1750 DO15
J5-20	Open Drain Out (0)	J5-1	Fixture ID (0)
J5-21	Open Drain Out (2)	J5-2	Fixture ID (2)
J5-22	Open Drain Out (4)	J5-3	Fixture ID (4)

Loopback Wire connection			
From		To	
Pin	Name	Pin	Name
J5-23	Open Drain Out (6)	J5-4	Fixture ID (6)
J5-68	Open Drain Out (1)	J5-49	Fixture ID (1)
J5-69	Open Drain Out (3)	J5-50	Fixture ID (3)
J5-70	Open Drain Out (5)	J5-51	Fixture ID (5)
J5-71	Open Drain Out (7)	J5-52	Fixture ID (7)
J5-6	Digital In (0)	J5-10	Spare_DigOut (0)
J5-7	Digital In (2)	J5-11	Spare_DigOut (2)
J5-8	Digital In (4)	J5-12	Spare_DigOut (4)
J5-9	Digital In (6)	J5-13	Spare_DigOut (6)
J5-54	Digital In (1)	J5-58	Spare_DigOut (1)
J5-55	Digital In (3)	J5-59	Spare_DigOut (3)
J5-56	Digital In (5)	J5-60	Spare_DigOut (5)
J5-57	Digital In (7)	J5-61	Spare_DigOut (7)
J6-24	interlock	J6-76	DCOM

Schematic for U8972-61628 CEDGN Load Card Cable



PINOUT for J1											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J1-1	row1	J3-1 & J3-9 & J3-17	J1-21		NC	J1-40		NC	J1-60		NC
J1-2	row2	J3-2 & J3-10 & J3-18	J1-22		NC	J1-41		NC	J1-61		NC
J1-3	row3	J3-3 & J3-11 & J3-19	J1-23		NC	J1-42		NC	J1-62		NC
J1-4	row4	J3-4 & J3-12 & J3-20	J1-24		NC	J1-43		NC	J1-63		NC
J1-5	row5	J3-5 & J3-13 & J4-1	J1-25		NC	J1-44		NC	J1-64		NC
J1-6	row6	J3-6 & J3-14 & J4-2	J1-26		NC	J1-45		NC	J1-65		NC
J1-7	row7	J3-7 & J3-15 & J4-3	J1-27		NC	J1-46		NC	J1-66		NC
J1-8	row8	J3-8 & J3-16 & J4-4	J1-28		NC	J1-47		NC	J1-67		NC
J1-9	row9	J3-41 & J3-49 & J3-57	J1-29		NC	J1-48		NC	J1-68		NC
J1-10	row10	J3-42 & J3-50 & J3-58	J1-30		NC	J1-49		NC	J1-69		NC
J1-11	row11	J3-43 & J3-51 & J3-59	J1-31		NC	J1-50		NC	J1-70		NC
J1-12	row12	J3-44 & J3-52 & J3-60	J1-32		NC	J1-51		NC	J1-71		NC
J1-13	row13	J3-45 & J3-53 & J4-49	J1-33		NC	J1-52		NC	J1-72		NC
J1-14	row14	J3-46 & J3-54 & J4-50	J1-34		NC	J1-53		NC	J1-73		NC
J1-15	row15	J3-47 & J3-55 & J4-51	J1-35		NC	J1-54		NC	J1-74		NC
J1-16	row16	J3-48 & J3-56 & J4-52	J1-36		NC	J1-55		NC	J1-75		NC
J1-17	row17	J4-5 & J4-7 & J4-9 & J4-11 & J4-13 & J4-15	J1-37		NC	J1-56		NC	J1-76		NC
J1-18	row18	J4-17 & J4-19 & J4-21 & J4-23 & J5-1 & J5-3	J1-38		NC	J1-57		NC	J1-77		NC
J1-19	row19	J5-5 & J5-7 & J5-9 & J5-11 & J5-13 & J5-15	J1-39		NC	J1-58		NC	J1-78		NC
J1-20	row20	J5-17 & J5-19 & J5-21 & J5-23 & J5-25 & J4-53				J1-59		NC			

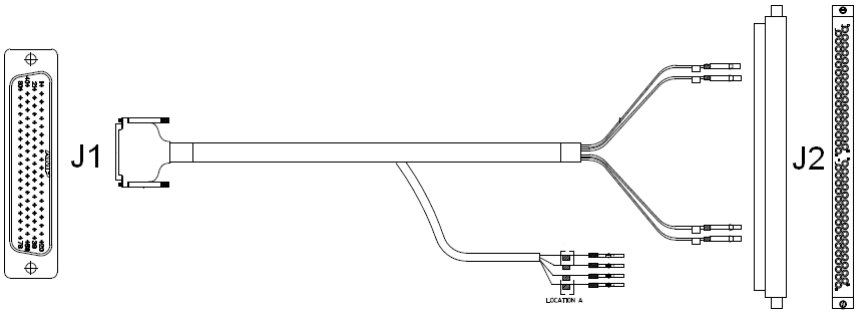
PINOUT for J2											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J2-1	row21	J4-55 & J4-57 & J4-59 & J4-61 & J4-63 & J4-65	J2-21		NC	J2-40		NC	J2-60		NC
J2-2	row22	J4-67 & J4-69 & J4-71 & J5-53 & J5-55 & J5-57	J2-22		NC	J2-41		NC	J2-61		NC
J2-3	row23	J5-59 & J5-61 & J5-63 & J5-65 & J5-67 & J5-69	J2-23		NC	J2-42		NC	J2-62		NC
J2-4	row24	J5-71 & J5-73 & J5-75 & J5-77 & J5-49 & J5-51	J2-24		NC	J2-43		NC	J2-63		NC
J2-5	row25	J4-6 & J4-8 & J4-10 & J4-12 & J4-14 & J4-16	J2-25		NC	J2-44		NC	J2-64		NC
J2-6	row26	J4-18 & J4-20 & J4-22 & J4-24 & J5-2 & J5-4	J2-26		NC	J2-45		NC	J2-65		NC
J2-7	row27	J5-6 & J5-8 & J5-10 & J5-12 & J5-14 & J5-16	J2-27		NC	J2-46		NC	J2-66		NC
J2-8	row28	J5-18 & J5-20 & J5-22 & J5-24 & J5-26 & J4-54	J2-28		NC	J2-47		NC	J2-67		NC
J2-9	row29	J4-56 & J4-58 & J4-60 & J4-62 & J4-64 & J4-66	J2-29		NC	J2-48		NC	J2-68		NC
J2-10	row30	J4-68 & J4-70 & J4-72 & J5-54 & J5-56 & J5-58	J2-30		NC	J2-49		NC	J2-69		NC
J2-11	row31	J5-60 & J5-62 & J5-64 & J5-66 & J5-68 & J5-70	J2-31		NC	J2-50		NC	J2-70		NC
J2-12	row32	J5-72& J5-74 & J5-76 & J5-78 & J5-50 & J5-52	J2-32		NC	J2-51		NC	J2-71		NC
J2-13	row33	Isense+ (4) SLU0	J2-33		NC	J2-52		NC	J2-72		NC
J2-14	row34	Isense- (4) SLU0	J2-34		NC	J2-53		NC	J2-73		NC
J2-15	row35	Isense+ (4) SLU1	J2-35		NC	J2-54		NC	J2-74		NC
J2-16	row36	Isense- (4) SLU1	J2-36		NC	J2-55		NC	J2-75		NC
J2-17		NC	J2-37		NC	J2-56		NC	J2-76		NC
J2-18		NC	J2-38		NC	J2-57		NC	J2-77		NC
J2-19		NC	J2-39		NC	J2-58		NC	J2-78		NC
J2-20		NC				J2-59		NC			

PINOUT for J3							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J3-1	LC16.Ch1	J3-21	NC	J3-40	NC	J3-60	LC16.Ch12
J3-2	LC16.Ch2	J3-22	NC	J3-41	LC16.Ch9	J3-61	NC
J3-3	LC16.Ch3	J3-23	NC	J3-42	LC16.Ch10	J3-62	NC
J3-4	LC16.Ch4	J3-24	NC	J3-43	LC16.Ch11	J3-63	NC
J3-5	LC16.Ch5	J3-25	NC	J3-44	LC16.Ch12	J3-64	NC
J3-6	LC16.Ch6	J3-26	NC	J3-45	LC16.Ch13	J3-65	NC
J3-7	LC16.Ch7	J3-27	NC	J3-46	LC16.Ch14	J3-66	NC
J3-8	LC16.Ch8	J3-28	NC	J3-47	LC16.Ch15	J3-67	NC
J3-9	LC16.Ch1	J3-29	NC	J3-48	LC16.Ch16	J3-68	NC
J3-10	LC16.Ch2	J3-30	NC	J3-49	LC16.Ch9	J3-69	NC
J3-11	LC16.Ch3	J3-31	NC	J3-50	LC16.Ch10	J3-70	NC
J3-12	LC16.Ch4	J3-32	NC	J3-51	LC16.Ch11	J3-71	NC
J3-13	LC16.Ch5	J3-33	NC	J3-52	LC16.Ch12	J3-72	NC
J3-14	LC16.Ch6	J3-34	NC	J3-53	LC16.Ch13	J3-73	NC
J3-15	LC16.Ch7	J3-35	NC	J3-54	LC16.Ch14	J3-74	NC
J3-16	LC16.Ch8	J3-36	NC	J3-55	LC16.Ch15	J3-75	NC
J3-17	LC16.Ch1	J3-37	NC	J3-56	LC16.Ch16	J3-76	NC
J3-18	LC16.Ch2	J3-38	NC	J3-57	LC16.Ch9	J3-77	NC
J3-19	LC16.Ch3	J3-39	NC	J3-58	LC16.Ch10	J3-78	NC
J3-20	LC16.Ch4			J3-59	LC16.Ch11		

PINOUT for J4							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J4-1	LC16.Ch5	J4-21	LC48.CH9	J4-40	NC	J4-60	LC48.CH27 Com
J4-2	LC16.Ch6	J4-22	LC48.CH9 Com	J4-41	NC	J4-61	LC48.CH28
J4-3	LC16.Ch7	J4-23	LC48.CH10	J4-42	NC	J4-62	LC48.CH28 Com
J4-4	LC16.Ch8	J4-24	LC48.CH10 Com	J4-43	NC	J4-63	LC48.CH29
J4-5	LC48.CH1	J4-25	NC	J4-44	NC	J4-64	LC48.CH29 Com
J4-6	LC48.CH1 Com	J4-26	NC	J4-45	NC	J4-65	LC48.CH30
J4-7	LC48.CH2	J4-27	NC	J4-46	NC	J4-66	LC48.CH30 Com
J4-8	LC48.CH2 Com	J4-28	NC	J4-47	NC	J4-67	LC48.CH31
J4-9	LC48.CH3	J4-29	NC	J4-48	NC	J4-68	LC48.CH31 Com
J4-10	LC48.CH3 Com	J4-30	NC	J4-49	LC16.Ch13	J4-69	LC48.CH32
J4-11	LC48.CH4	J4-31	NC	J4-50	LC16.Ch14	J4-70	LC48.CH32 Com
J4-12	LC48.CH4 Com	J4-32	NC	J4-51	LC16.Ch15	J4-71	LC48.CH33
J4-13	LC48.CH5	J4-33	NC	J4-52	LC16.Ch16	J4-72	LC48.CH33 Com
J4-14	LC48.CH5 Com	J4-34	NC	J4-53	LC48.CH24	J4-73	NC
J4-15	LC48.CH6	J4-35	NC	J4-54	LC48.CH24 Com	J4-74	NC
J4-16	LC48.CH6 Com	J4-36	NC	J4-55	LC48.CH25	J4-75	NC
J4-17	LC48.CH7	J4-37	NC	J4-56	LC48.CH25 Com	J4-76	NC
J4-18	LC48.CH7 Com	J4-38	NC	J4-57	LC48.CH26	J4-77	NC
J4-19	LC48.CH8	J4-39	NC	J4-58	LC48.CH26 Com	J4-78	NC
J4-20	LC48.CH8 Com			J4-59	LC48.CH27		

PINOUT for J5							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J5-1	LC48.CH11	J5-21	LC48.CH21	J5-40	NC	J5-60	LC48.CH37 Com
J5-2	LC48.CH11 Com	J5-22	LC48.CH21 Com	J5-41	NC	J5-61	LC48.CH38
J5-3	LC48.CH12	J5-23	LC48.CH22	J5-42	NC	J5-62	LC48.CH38 Com
J5-4	LC48.CH12 Com	J5-24	LC48.CH22 Com	J5-43	NC	J5-63	LC48.CH39
J5-5	LC48.CH13	J5-25	LC48.CH23	J5-44	NC	J5-64	LC48.CH39 Com
J5-6	LC48.CH13 Com	J5-26	LC48.CH23 Com	J5-45	NC	J5-65	LC48.CH40
J5-7	LC48.CH14	J5-27	NC	J5-46	NC	J5-66	LC48.CH40 Com
J5-8	LC48.CH14 Com	J5-28	NC	J5-47	NC	J5-67	LC48.CH41
J5-9	LC48.CH15	J5-29	NC	J5-48	NC	J5-68	LC48.CH41 Com
J5-10	LC48.CH15 Com	J5-30	NC	J5-49	LC48.CH47	J5-69	LC48.CH42
J5-11	LC48.CH16	J5-31	NC	J5-50	LC48.CH47 Com	J5-70	LC48.CH42 Com
J5-12	LC48.Ch16 Com	J5-32	NC	J5-51	LC48.CH48	J5-71	LC48.CH43
J5-13	LC48.CH17	J5-33	NC	J5-52	LC48.CH48 Com	J5-72	LC48.CH43 Com
J5-14	LC48.CH17 Com	J5-34	NC	J5-53	LC48.CH34	J5-73	LC48.CH44
J5-15	LC48.CH18	J5-35	NC	J5-54	LC48.CH34 Com	J5-74	LC48.CH 44 Com
J5-16	LC48.CH18 Com	J5-36	NC	J5-55	LC48.CH35	J5-75	LC48.CH45
J5-17	LC48.CH19	J5-37	NC	J5-56	LC48.CH35 Com	J5-76	LC48.CH45 Com
J5-18	LC48.CH19 Com	J5-38	NC	J5-57	LC48.CH36	J5-77	LC48.CH46
J5-19	LC48.CH20	J5-39	NC	J5-58	LC48.CH36 Com	J5-78	LC48.CH46 Com
J5-20	LC48.CH20 Com			J5-59	LC48.CH37		

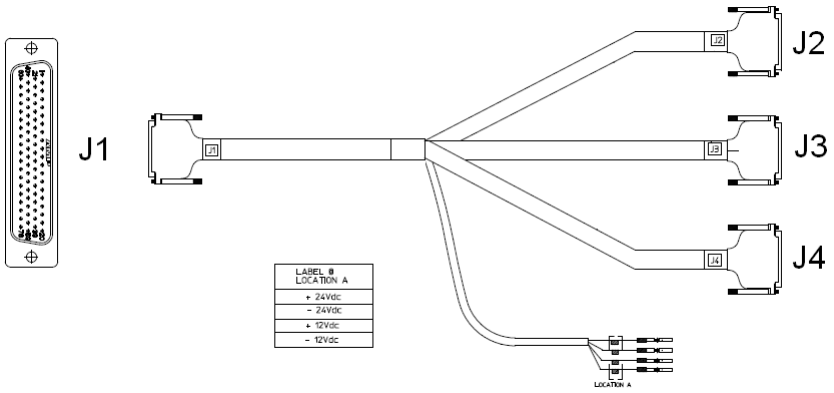
Schematic for U8972-61629 CEDGN Heavy Duty Load Card Cable



PINOUT for J1											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J1-1	row1	J2-A-1 & J2-A-17 & J2-B-1 & J2-B-17	J1-21		NC	J1-40		NC	J1-60		NC
J1-2	row2	J2-A-2 & J2-A-18 & J2-B-2 & J2-B-18	J1-22		NC	J1-41		NC	J1-61		NC
J1-3	row3	J2-A-3 & J2-A-19 & J2-B-3 & J2-B-19	J1-23		NC	J1-42		NC	J1-62		NC
J1-4	row4	J2-A-4 & J2-A-20& J2-B-4 & J2-B-20	J1-24		NC	J1-43		NC	J1-63		NC
J1-5	row5	J2-A-5 & J2-A-21 & J2-B-5 & J2-B-21	J1-25		NC	J1-44		NC	J1-64		NC
J1-6	row6	J2-A-6 & J2-A-22 & J2-B-6 & J2-B-22	J1-26		NC	J1-45		NC	J1-65		NC
J1-7	row7	J2-A-7 & J2-A-23 & J2-B-7 & J2-B-23	J1-27		NC	J1-46		NC	J1-66		NC
J1-8	row8	J2-A-8 & J2-A-24 & J2-B-8 & J2-B-24	J1-28		NC	J1-47		NC	J1-67		NC
J1-9	row9	J2-A-9 & J2-A-25 & J2-B-9 & J2-B-25	J1-29		NC	J1-48		NC	J1-68		NC
J1-10	row10	J2-A-10 & J2-A-26 & J2-B-10 & J2-B-26	J1-30		NC	J1-49		NC	J1-69		NC
J1-11	row11	J2-A-11 & J2-A-27 & J2-B-11 & J2-B-27	J1-31		NC	J1-50		NC	J1-70		NC
J1-12	row12	J2-A-12 & J2-A-28 & J2-B-12 & J2-B-28	J1-32		NC	J1-51		NC	J1-71		NC
J1-13	row13	J2-A-13 & J2-A-29 & J2-B-13 & J2-B-29	J1-33		NC	J1-52		NC	J1-72		NC
J1-14	row14	J2-A-14 & J2-A-30 & J2-B-14 & J2-B-30	J1-34		NC	J1-53		NC	J1-73		NC
J1-15	row15	J2-A-15 & J2-A-31 & J2-B-15 & J2-B-31	J1-35		NC	J1-54		NC	J1-74		NC
J1-16	row16	J2-A-16 & J2-A-32 & J2-B-16 & J2-B-32	J1-36		NC	J1-55		NC	J1-75		NC
J1-17	row17	Isense+ (4) SLU0	J1-37		NC	J1-56		NC	J1-76		NC
J1-18	row18	Isense- (4) SLU0	J1-38		NC	J1-57		NC	J1-77		NC
J1-19	row19	Isense+ (4) SLU1	J1-39		NC	J1-58		NC	J1-78		NC
J1-20	row20	Isense- (4) SLU1				J1-59		NC			

Pinout for J2			
Connector A			
1	CH1	17	CH1
2	CH2	18	CH2
3	CH3	19	CH3
4	CH4	20	CH4
5	CH5	21	CH5
6	CH6	22	CH6
7	CH7	23	CH7
8	CH8	24	CH8
9	CH9	25	CH9
10	CH10	26	CH10
11	CH11	27	CH11
12	CH12	28	CH12
13	CH13	29	CH13
14	CH14	30	CH14
15	CH15	31	CH15
16	CH16	32	CH16
Connector B			
1	CH1	17	CH1
2	CH2	18	CH2
3	CH3	19	CH3
4	CH4	20	CH4
5	CH5	21	CH5
6	CH6	22	CH6
7	CH7	23	CH7
8	CH8	24	CH8
9	CH9	25	CH9
10	CH10	26	CH10
11	CH11	27	CH11
12	CH12	28	CH12
13	CH13	29	CH13
14	CH14	30	CH14
15	CH15	31	CH15
16	CH16	32	CH16

Schematic for U8972-61630 CEDGN E-Load Cable



PINOUT for J1											
PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to	PIN	Name	Connect to
J1-1	row21	J2-21 & J4-55	J1-21		NC	J1-40		NC	J1-60		NC
J1-2	row22	J2-22 & J4-56	J1-22		NC	J1-41		NC	J1-61		NC
J1-3	row23	J2-24 & J4-58	J1-23		NC	J1-42		NC	J1-62		NC
J1-4	row24	J2-25 & J4-59	J1-24		NC	J1-43		NC	J1-63		NC
J1-5	row25	J2-30 & J4-64	J1-25	UUTCom	J2-23 & J4-57	J1-44		NC	J1-64		NC
J1-6	row26	J2-31 & J4-65	J1-26	UUTCom	J2-26 & J4-60	J1-45		NC	J1-65		NC
J1-7	row27	J2-33 & J4-67	J1-27	UUTCom	J2-29 & J4-63	J1-46		NC	J1-66		NC
J1-8	row28	J2-35 & J4-69	J1-28	UUTCom	J2-32 & J4-66	J1-47		NC	J1-67		NC
J1-9	row29	J2-36 & J4-70	J1-29	UUTCom	J2-34 & J4-68	J1-48		NC	J1-68		NC
J1-10	row30	J2-38 & J4-72	J1-30	UUTCom	J2-37 & J4-71	J1-49		NC	J1-69		NC
J1-11	row31	J2-39 & J4-73	J1-31	UUTCom	J2-40 & J4-74	J1-50		NC	J1-70		NC
J1-12	row32	J3-25 & J4-75	J1-32	UUTCom	J3-26 & J4-76	J1-51		NC	J1-71		NC
J1-13	row33	J3-27 & J4-77	J1-33		NC	J1-52		NC	J1-72		NC
J1-14	row34	J3-28 & J4-78	J1-34		NC	J1-53		NC	J1-73		NC
J1-15	row35	+24Vdc Supply	J1-35		NC	J1-54		NC	J1-74		NC
J1-16	row36	-24Vdc Supply	J1-36		NC	J1-55		NC	J1-75		NC
J1-17	row37	+12Vdc Supply	J1-37		NC	J1-56		NC	J1-76		NC
J1-18	row38	-12Vdc Supply	J1-38		NC	J1-57		NC	J1-77		NC
J1-19	row39	NC	J1-39		NC	J1-58		NC	J1-78		NC
J1-20	row40	NC				J1-59		NC			

PINOUT for J2							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J2-1	NC	J2-21	TRIG_IN	J2-40	CH2-A7	J2-60	NC
J2-2	NC	J2-22	TRIG_OUT	J2-41	NC	J2-61	NC
J2-3	NC	J2-23	TRIG_GND	J2-42	NC	J2-62	NC
J2-4	NC	J2-24	DIG1	J2-43	NC	J2-63	NC
J2-5	NC	J2-25	DIG2	J2-44	NC	J2-64	NC
J2-6	NC	J2-26	DIG_GND	J2-45	NC	J2-65	NC
J2-7	NC	J2-27	NC	J2-46	NC	J2-66	NC
J2-8	NC	J2-28	NC	J2-47	NC	J2-67	NC
J2-9	NC	J2-29	CH1-A4	J2-48	NC	J2-68	NC
J2-10	NC	J2-30	CH1-A5	J2-49	NC	J2-69	NC
J2-11	NC	J2-31	CH1-A6	J2-50	NC	J2-70	NC
J2-12	NC	J2-32	CH1-A7	J2-51	NC	J2-71	NC
J2-13	NC	J2-33	CH1-A8	J2-52	NC	J2-72	NC
J2-14	NC	J2-34	CH1-A9	J2-53	NC	J2-73	NC
J2-15	NC	J2-35	CH1-A10	J2-54	NC	J2-74	NC
J2-16	NC	J2-36	CH1-A11	J2-55	NC	J2-75	NC
J2-17	NC	J2-37	CH2-A4	J2-56	NC	J2-76	NC
J2-18	NC	J2-38	CH2-A5	J2-57	NC	J2-77	NC
J2-19	NC	J2-39	CH2-A6	J2-58	NC	J2-78	NC
J2-20	NC			J2-59	NC		

PINOUT for J3							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J3-1	NC	J3-21	NC	J3-40	NC	J3-60	NC
J3-2	NC	J3-22	NC	J3-41	NC	J3-61	NC
J3-3	NC	J3-23	NC	J3-42	NC	J3-62	NC
J3-4	NC	J3-24	NC	J3-43	NC	J3-63	NC
J3-5	NC	J3-25	CH2-A8	J3-44	NC	J3-64	NC
J3-6	NC	J3-26	CH2-A9	J3-45	NC	J3-65	NC
J3-7	NC	J3-27	CH2-A10	J3-46	NC	J3-66	NC
J3-8	NC	J3-28	CH2-A11	J3-47	NC	J3-67	NC
J3-9	NC	J3-29	NC	J3-48	NC	J3-68	NC
J3-10	NC	J3-30	NC	J3-49	NC	J3-69	NC
J3-11	NC	J3-31	NC	J3-50	NC	J3-70	NC
J3-12	NC	J3-32	NC	J3-51	NC	J3-71	NC
J3-13	NC	J3-33	NC	J3-52	NC	J3-72	NC
J3-14	NC	J3-34	NC	J3-53	NC	J3-73	NC
J3-15	NC	J3-35	NC	J3-54	NC	J3-74	NC
J3-16	NC	J3-36	NC	J3-55	NC	J3-75	NC
J3-17	NC	J3-37	NC	J3-56	NC	J3-76	NC
J3-18	NC	J3-38	NC	J3-57	NC	J3-77	NC
J3-19	NC	J3-39	NC	J3-58	NC	J3-78	NC
J3-20	NC			J3-59	NC		

PINOUT for J4							
PIN	Name	PIN	Name	PIN	Name	PIN	Name
J4-1	NC	J4-21	NC	J4-40	NC	J4-60	DIG_GND
J4-2	NC	J4-22	NC	J4-41	NC	J4-61	NC
J4-3	NC	J4-23	NC	J4-42	NC	J4-62	NC
J4-4	NC	J4-24	NC	J4-43	NC	J4-63	CH1-A4
J4-5	NC	J4-25	NC	J4-44	NC	J4-64	CH1-A5
J4-6	NC	J4-26	NC	J4-45	NC	J4-65	CH1-A6
J4-7	NC	J4-27	NC	J4-46	NC	J4-66	CH1-A7
J4-8	NC	J4-28	NC	J4-47	NC	J4-67	CH1-A8
J4-9	NC	J4-29	NC	J4-48	NC	J4-68	CH1-A9
J4-10	NC	J4-30	NC	J4-49	NC	J4-69	CH1-A10
J4-11	NC	J4-31	NC	J4-50	NC	J4-70	CH1-A11
J4-12	NC	J4-32	NC	J4-51	NC	J4-71	CH2-A4
J4-13	NC	J4-33	NC	J4-52	NC	J4-72	CH2-A5
J4-14	NC	J4-34	NC	J4-53	NC	J4-73	CH2-A6
J4-15	NC	J4-35	NC	J4-54	NC	J4-74	CH2-A7
J4-16	NC	J4-36	NC	J4-55	TRIG_IN	J4-75	CH2-A8
J4-17	NC	J4-37	NC	J4-56	TRIG_OUT	J4-76	CH2-A9
J4-18	NC	J4-38	NC	J4-57	TRIG_GND	J4-77	CH2-A10
J4-19	NC	J4-39	NC	J4-58	DIG1	J4-78	CH2-A11
J4-20	NC			J4-59	DIG2		

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